



0.75 inch OLED Display Series



GDOR0075W

Dalian Good Display Co., Ltd.

REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	■ INITIAL RELEASE	2015. 12. 15	
X02	■ Add the panel electrical specifications ■ Add the lifetime specifications ■ Add the application circuit	2016. 01. 07	Page 6, 7, 8 & 16

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1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by GooDisplay. This document, together with the Module Assembly Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications.

3. FEATURES

- Circular
- Small molecular organic light emitting diode.
- Color : White
- 16 gray scale.
- Panel resolution : 128x128
- Driver IC : SSD1327
- Excellent Quick response time : 10 μ s
- Extremely thin thickness for best mechanism design : 1.21 mm
- High contrast : 2000:1
- Wide viewing angle : 160°
- Strong environmental resistance.
- Serial Peripheral Interface, I²C Interface.
- Wide range of operating temperature : -40 to 70°C
- Anti-glare polarizer.

3. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128 x 128	dot
2	Dot Size	0.13 (W) x 0.13 (H)	mm ²
3	Dot Pitch	0.15 (W) x 0.15 (H)	mm ²
4	Aperture Rate	75	%
5	Active Area	D=19.18	mm
6	Panel Size	23.15 (W) x 25.93 (H)	mm ²
7*	Panel Thickness	1.02 ± 0.15	mm
8	Module Size	23.15 (W) x 40.93 (H) x 1.21 (T)	mm ³
9	Diagonal A/A size	0.75	inch
10	Module Weight	0.05	gram

* Panel thickness includes substrate glass, cover glass and UV glue thickness.

4. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V_{CI})	-0.3	4	V	$T_a = 25^\circ\text{C}$	IC maximum rating
Supply Voltage (V_{CC})	8	19	V	$T_a = 25^\circ\text{C}$	IC maximum rating
Operating Temp.	-40	70	$^\circ\text{C}$	-	-
Storage Temp	-40	85	$^\circ\text{C}$	-	Note (2)

Note:

- (1) Maximum ratings are those values beyond which damages to the OLED module may occur. The OLED functional operation should be restricted to the limits in the section 6. Electrical Characteristics tables.
- (2) The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C .

5. ELECTRICAL CHARACTERISTICS

5.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Driver power supply (for OLED panel)	$T_a = 25^\circ\text{C}$	13.5	14	14.5	V
V_{CI}	Low voltage power supply (Table 6.1)	$T_a = 25^\circ\text{C}$	1.65	-	3.5	V
V_{DD}	Logic Supply Voltage		1.65		2.6	V
V_{OH}	High logic output level	$I_{out}=100\mu\text{A}$,	$0.9 \cdot V_{CI}$	-	V_{CI}	V
V_{OL}	Low logic output level	$I_{out}=100\mu\text{A}$,	0	-	$0.1 \cdot V_{CI}$	V
V_{IH}	High logic input level	$I_{out}=100\mu\text{A}$,	$0.8 \cdot V_{CI}$	-	V_{CI}	V
V_{IL}	Low logic input level	$I_{out}=100\mu\text{A}$,	0	-	$0.2 \cdot V_{CI}$	V

Table 5.1

V_{CI}	V_{DD}	Remark
1.65 V ~ 2.6V	1.65V ~ 2.6V	V_{DD} should be tied to V_{CI} and supplied by external power source
2.6V ~ 3.5V	2.4V ~ 2.6V	V_{DD} is regulated from V_{CI}

5.2 ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current consumption (ICC)	-	17	18	mA	All pixels on (1)
	-	3	4	mA	20% pixels on (1)
Standby mode current consumption (ICC)	-	1	2	mA	Standby mode 10% pixels on (2)
Normal mode power consumption	-	238	252	mW	All pixels on (1)
	-	42	56	mW	20% pixels on (1)
Standby mode power consumption	-	14	28	mW	Standby mode 10% pixels on (2)
ICI sleep mode current (Enable Internal VDD)	-	-	60	uA	Sleep mode Current (3)
ICI sleep mode current (Disable Internal VDD)	-	-	10	uA	Sleep mode Current (3)
ICC sleep mode current	-	-	10	uA	Sleep mode Current (3)
Pixel Luminance	60	80		cd/m ²	Display Average
Standby Luminance		20		cd/m ²	
CIE _x (White)	0.26	0.30	0.34		CIE1931
CIE _y (White)	0.29	0.33	0.37		CIE1931
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		μs	

(1) Normal mode condition :

- Driving Voltage : 14V
- Contrast setting : 0x53
- Frame rate : 105Hz
- Duty setting : 1/128

(2) Standby mode condition :

- Driving Voltage : 14V
- Contrast setting : 0x10
- Frame rate : 105Hz
- Duty setting : 1/128

(3) Sleep mode condition :

When send 0xae command OLED display off and memory data will be maintained (Disable Internal VDD during Sleep mode).

(4) Wake up condition :

When send 0xaf command OLED will be turned on.

6. LIFETIME SPECIFICATION

ITEM	MIN	UNIT	Condition	Remark
Life Time	10,000	Hrs	100 cd/m ² , 50% checkerboard	Note (1)
Life Time	12,000	Hrs	80 cd/m ² , 50% checkerboard	Note (2)
Life Time	16,000	Hrs	60 cd/m ² , 50% checkerboard	Note (3)

Note:

(A) Under $V_{cc} = 14V$, $T_a = 25^\circ C$, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 100 cd/m² :

- Contrast setting : 0x6d
- Frame rate : 105Hz
- Duty setting : 1/128

(2) Setting of 80 cd/m² :

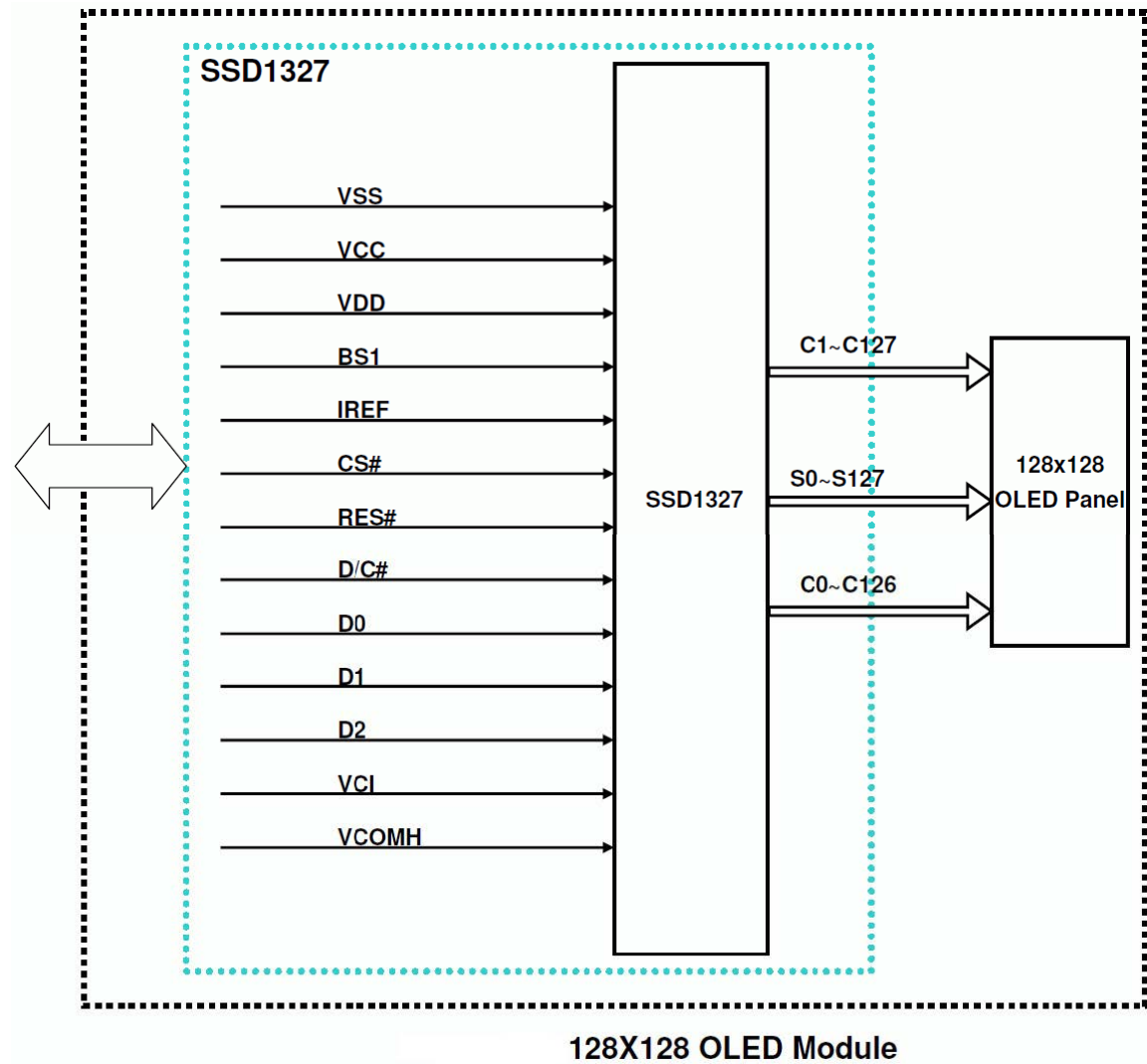
- Contrast setting : 0x53
- Frame rate : 105Hz
- Duty setting : 1/128

(3) Setting of 60 cd/m² :

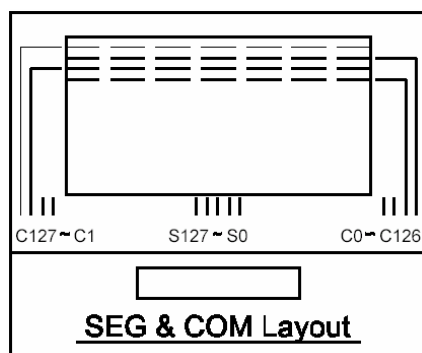
- Contrast setting : 0x3a
- Frame rate : 105Hz
- Duty setting : 1/128

7. INTERFACE

7.1 FUNCTION BLOCK DIAGRAM



7.2 PANEL LAYOUT DIAGRAM



7.3 PIN ASSIGNMENTS

PIN NAME	PIN NO.	DESCRIPTION
VSS	1	Ground pin.
VCC	2	Power supply for panel driving voltage.
VDD	3	Power supply pin for core logic operation. VDD can be supplied externally (within the range of 2.4V to 2.6V) or regulated internally from VCI. A capacitor should be connected between VDD and VSS under all circumstances.
BS1	4	MCU bus interface selection pins. I ² C(BS1=1);SPI(BS1=0).
VSS	5	Ground pin.
IREF	6	This pin is the segment output current reference pin. A resistor should be connected between this pin and VSS.
CS#	7	This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW (active LOW).
RES#	8	This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed.
D/C#	9	This pin is Data/Command control pin connecting to the MCU.
D0	10	When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN and D2 should be kept NC. When I ² C mode is selected, D2, D1 should be tied together and serve as SDAout,SDAin in application and D0 is the serial clock input, SCL.
D1	11	
D2	12	
VCI	13	Low voltage power supply and power supply for interface logic level. It should match with the MCU interface voltage level and must be connected to external source. (Regulated internally from VCI when VCI is >2.6V)
VCOMH	14	COM signal deselected voltage level. A capacitor should be connected between this pin and VSS.
VCC	15	Power supply for panel driving voltage.

7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128x128x4 bits. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. The GDDRAM address maps below tables show some examples on using the command “Set Re-map” A0h to re-map the GDDRAM. In the following tables, the lower nibble and higher nibble of D0, D1, D2 ... D8189, D8190, D8191 represent the 128x128 data bytes in the GDDRAM.

The GDDRAM map under the following condition:

- Command “Set Re-map” A0h is set to:
 - Disable Column Address Re-map (A[0]=0)
 - Disable Nibble Re-map (A[1]=0)
 - Enable Horizontal Address Increment (A[2]=0)
 - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 ... D8191

GDDRAM address map 1

		SEG0	SEG1	SEG2	SEG3		SEG124	SEG125	SEG126	SEG127	SEG Outputs Column Address (HEX)
		00		01			3E		3F		
COM0	00	D0[3:0]	D0[7:4]	D1[3:0]	D1[7:4]		D62[3:0]	D62[7:4]	D63[3:0]	D63[7:4]	
COM1	01	D64[3:0]	D64[7:4]	D65[3:0]	D65[7:4]		D126[3:0]	D126[7:4]	D127[3:0]	D127[7:4]	
COM126	7E	D8064[3:0]	D8064[7:4]	D8065[3:0]	D8065[7:4]		D8126[3:0]	D8126[7:4]	D8127[3:0]	D8127[7:4]	
COM127	7F	D8128[3:0]	D8128[7:4]	D8129[3:0]	D8129[7:4]		D8190[3:0]	D8190[7:4]	D8191[3:0]	D8191[7:4]	

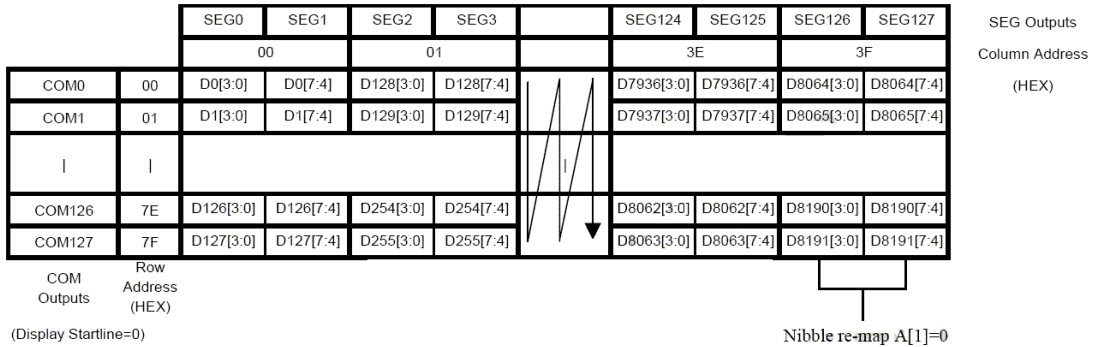
COM Outputs Row Address (HEX)

Nibble re-map A[1]=0

The GDDRAM map under the following condition:

- Command “Set Re-map” A0h is set to:
 - Disable Column Address Re-map (A[0]=0)
 - Disable Nibble Re-map (A[1]=0)
 - Enable Vertical Address Increment (A[2]=1)
 - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 ... D8191

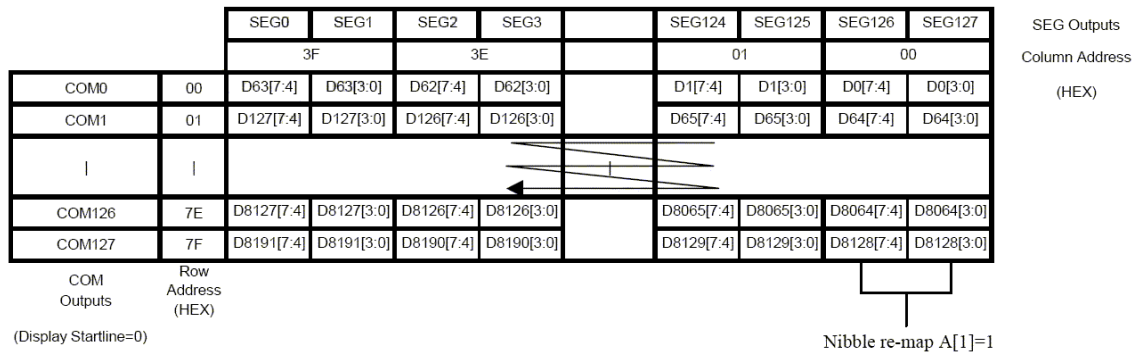
GDDRAM address map 2



The GDDRAM map under the following condition:

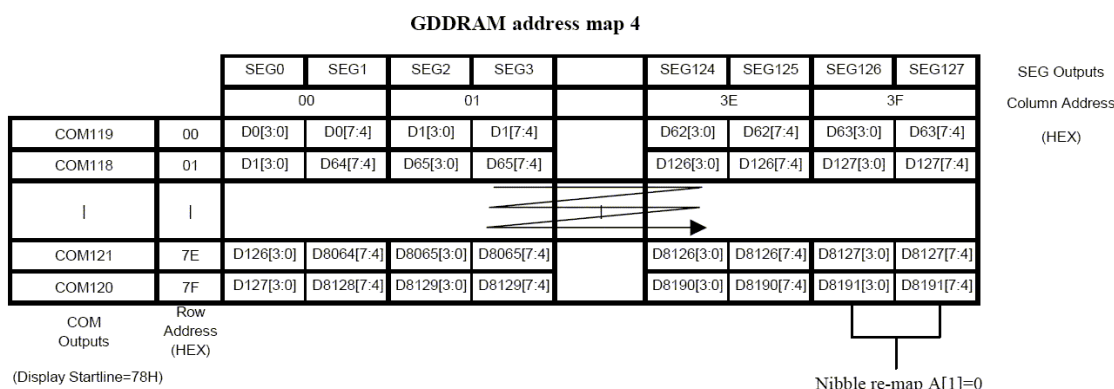
- Command “Set Re-map” A0h is set to:
 - Enable Column Address Re-map (A[0]=1)
 - Enable Nibble Re-map (A[1]=1)
 - Enable Horizontal Address Increment (A[2]=0)
 - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Data byte sequence: D0, D1, D2 ... D8191

GDDRAM address map 3



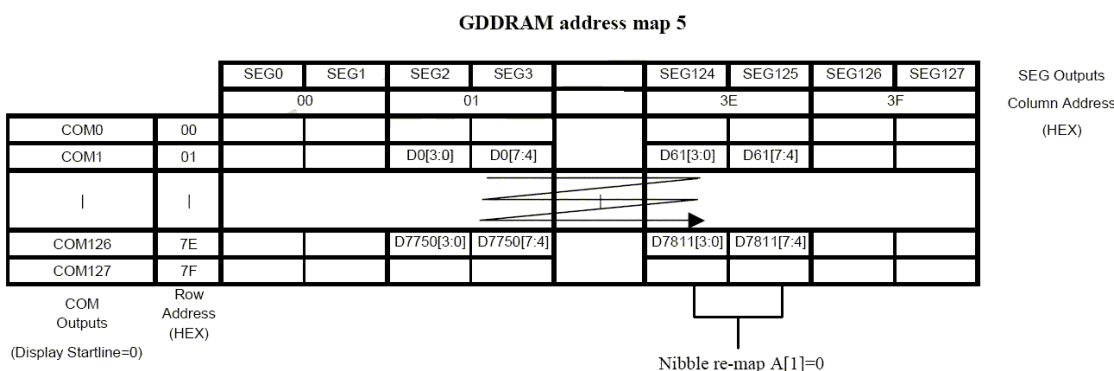
The example in which the display start line register is set to 10h with the following condition:

- Command “Set Re-map” A0h is set to:
 - Disable Column Address Re-map (A[0]=0)
 - Disable Nibble Re-map (A[1]=0)
 - Enable Horizontal Address Increment (A[2]=0)
 - Enable COM Re-map (A[4]=1)
- Display Start Line=78h (corresponds to COM119)
- Data byte sequence: D0, D1, D2 ... D8191



The GDDRAM map under the following condition:

- Command “Set Re-map” A0h is set to:
 - Disable Column Address Re-map (A[0]=0)
 - Disable Nibble Re-map (A[1]=0)
 - Enable Horizontal Address Increment (A[2]=0)
 - Disable COM Re-map (A[4]=0)
- Display Start Line=00h
- Column Start Address=01h
- Column End Address=3Eh
- Row Start Address=01h
- Row End Address=7Eh
- Data byte sequence: D0, D1, D2 ... D7811



7.5 INTERFACE TIMING CHART

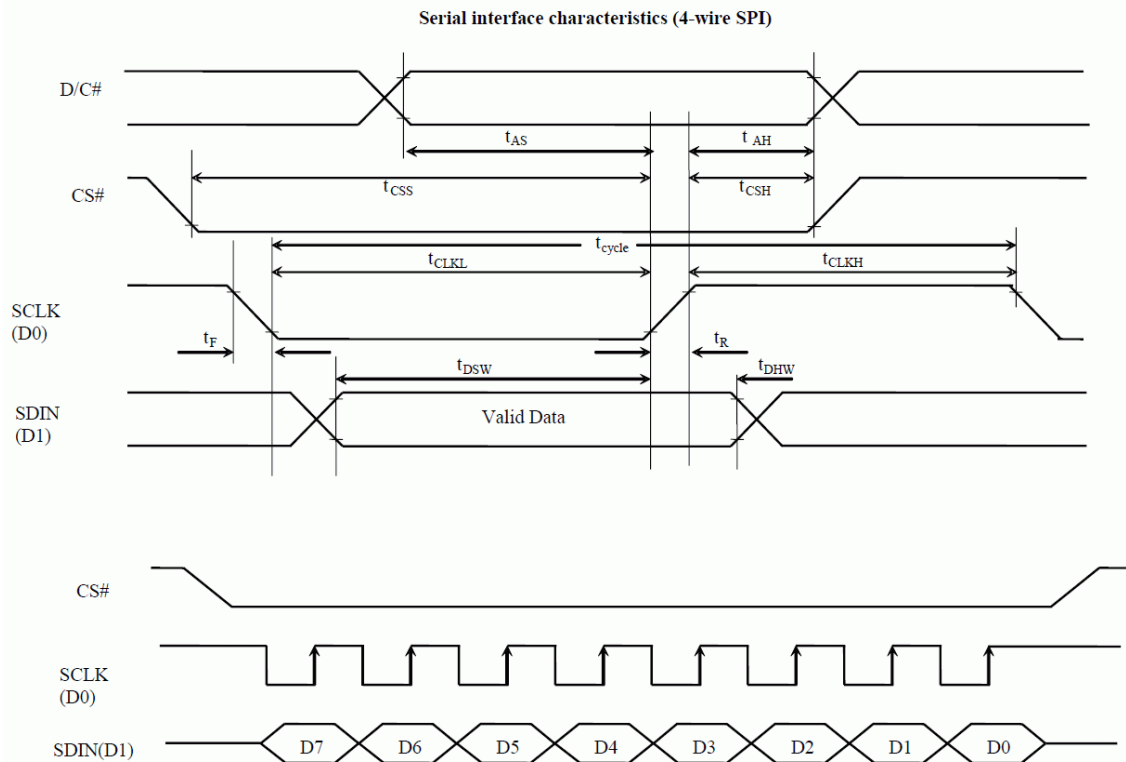
Serial Interface Timing Characteristics (4-wire SPI)

$V_{CI} - V_{SS} = 1.65V$ to $2.1V$ ($T_A = 25^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	220	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	30	-	-	ns
t_{CLKL}	Clock Low Time	25	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

$V_{CI} - V_{SS} = 2.1V$ to $3.5V$ ($T_A = 25^\circ C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	160	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns



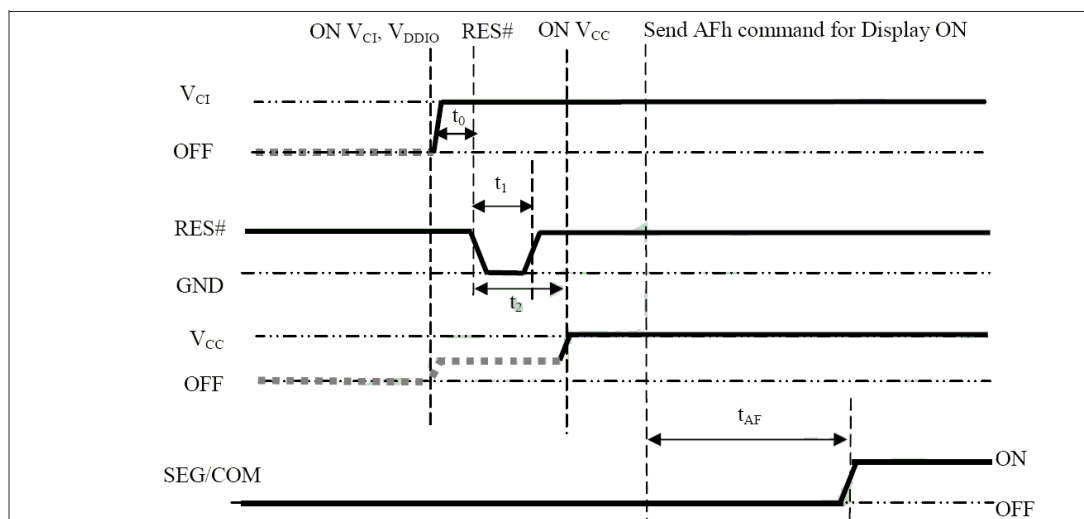
8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

8.1 POWER ON / OFF SEQUENCE

Power ON sequence:

1. Power ON V_{CI} .
2. After V_{CI} becomes stable, set wait time at least 1ms (t_0) for internal V_{DD} become stable. Then set RES# pin LOW (logic low) for at least 100us (t_1)⁽⁴⁾ and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 100us (t_2). Then Power ON V_{CC} .⁽¹⁾
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms(t_{AF}).

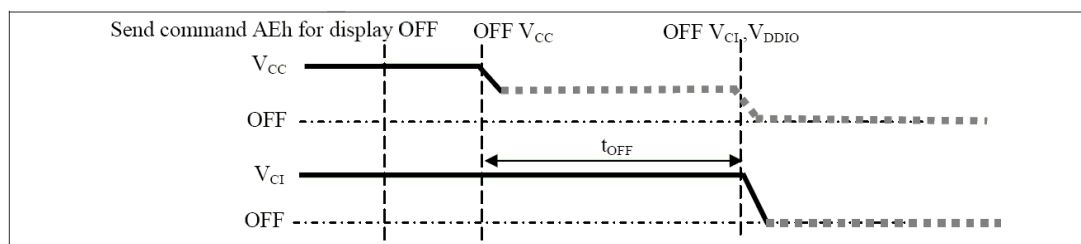
The Power ON sequence.



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC} .^{(1), (2), (3)}
3. Wait for t_{OFF} . Power OFF V_{CI} . (where Minimum $t_{OFF}=80ms$ ⁽⁵⁾, Typical $t_{OFF}=100ms$)

The Power OFF sequence

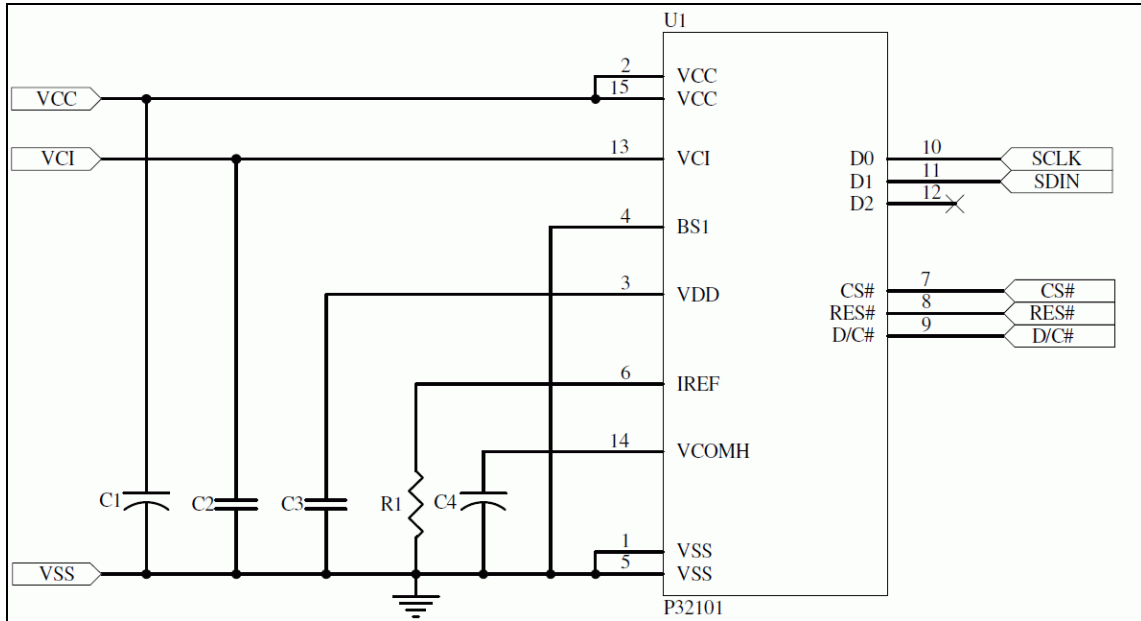


Note:

- (1) Since an ESD protection circuit is connected between V_{CI} and V_{CC} , V_{CC} becomes lower than V_{CI} whenever V_{CI} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.
- (2) V_{CC} should be kept disable when it is OFF.
- (3) Power pins (V_{CI} , V_{CC}) can never be pulled to ground under any circumstance.
- (4) The register values are reset after t_1 .
- (5) V_{CI} should not be Power OFF before V_{CC} Power OFF

8.2 APPLICATION CIRCUIT

(Internal VDD: VCI =2.6V~3.5V)



Recommend components:

C1, C4: 4.7uF/35V(Tantalum type) or VISHAY (572D475X0025A2T)

C2, C3: 1uF/16V(0603)

R1: 1M ohm 1%(0603)

This circuit is for SPI interface.

8.3 COMMAND TABLE

Refer to IC Spec.: SSD1327

9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85 °C, 240hrs	5
2	High temp. (Operation)	70 °C, 120hrs	5
3	Low temp. (Operation)	-40 °C, 120hrs	5
4	High temp. / High humidity (Operation)	65 °C, 90%RH, 120hrs	5
5	Thermal shock (Non-operation)	-40 °C ~85 °C (-40 °C /30min; transit /3min; 85 °C /30min; transit /3min) 1cycle: 66min, 100 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle 、 3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1, 4 & 5.

Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within \pm 50% of initial value.

11. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time T_r is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time T_f is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

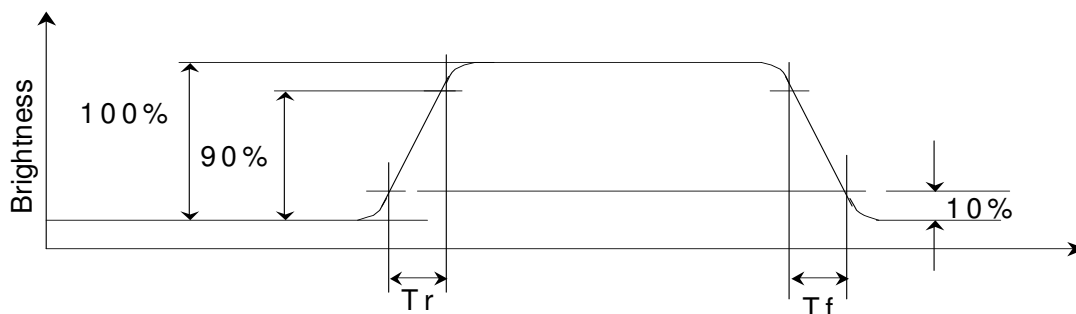


Figure 2 Response time

D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

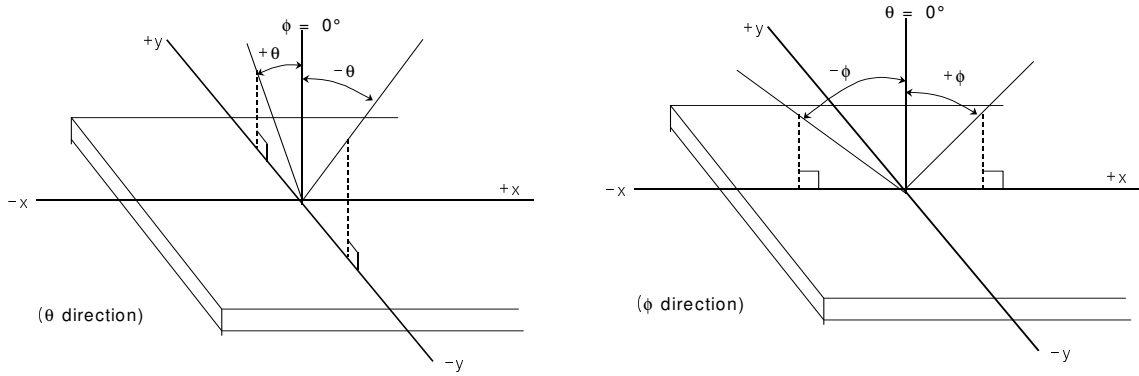
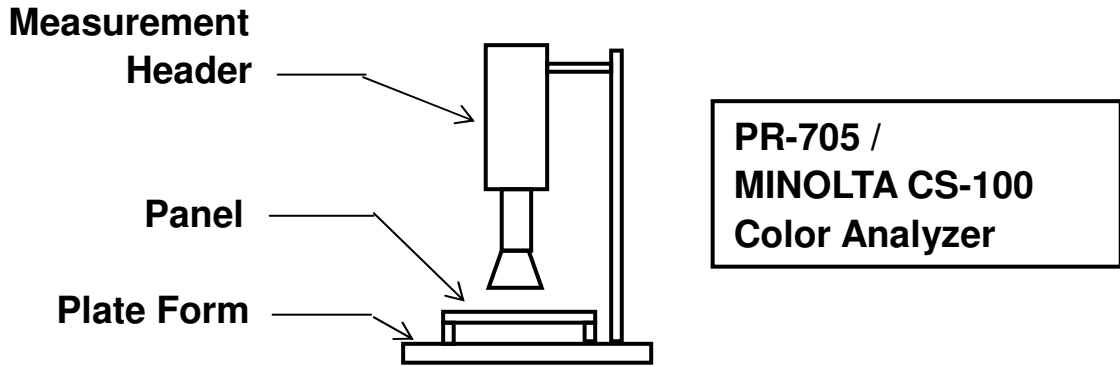


Figure 3 Viewing angle

APPENDIX 2: MEASUREMENT APPARATUS

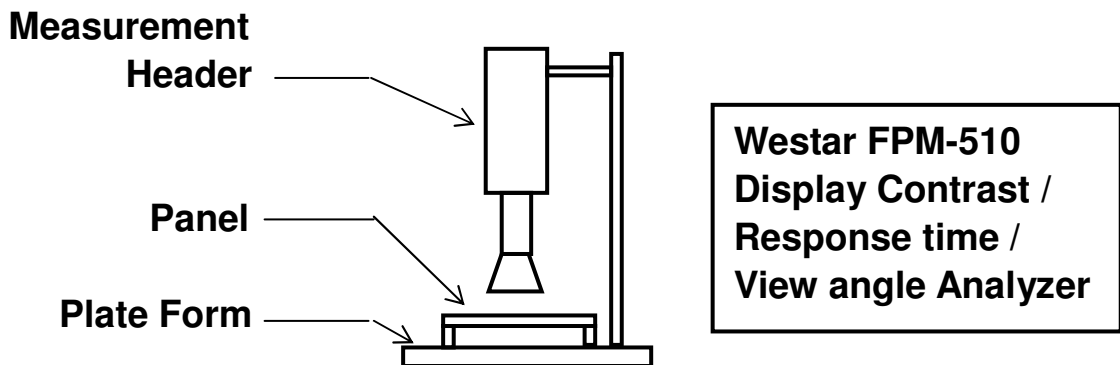
A. LUMINANCE/COLOR COORDINATE

PHOTO RESEARCH PR-705, MINOLTA CS-100

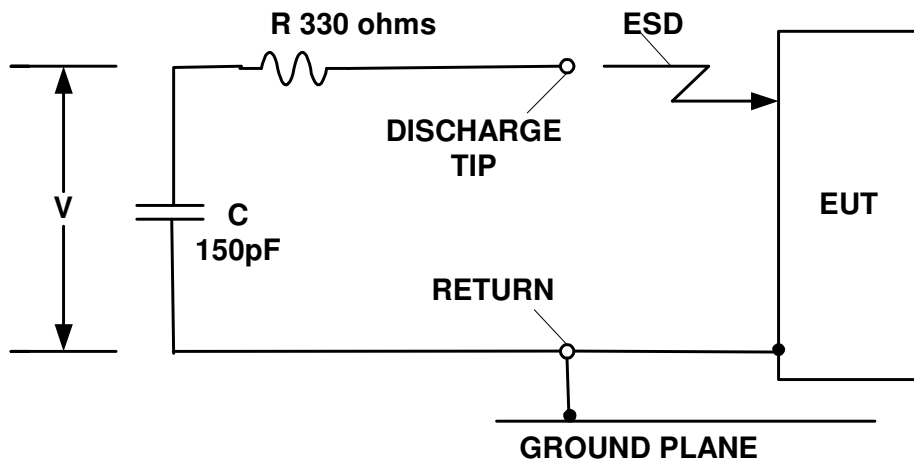


B. CONTRAST / RESPONSE TIME / VIEWING ANGLE

WESTAR CORPORATION FPM-510



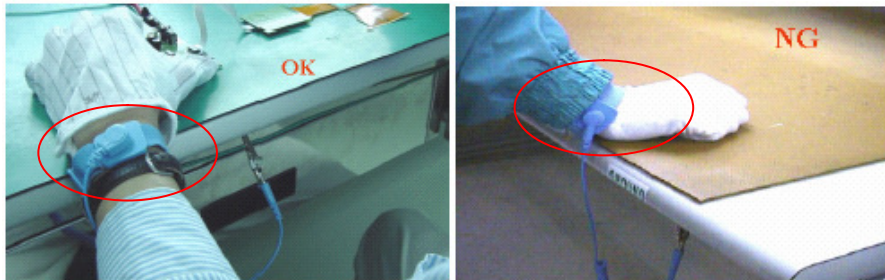
C. ESD ON AIR DISCHARGE MODE



APPENDIX 3: PRECAUTIONS FOR USING THE OLED MODULE

Precautions for Handling

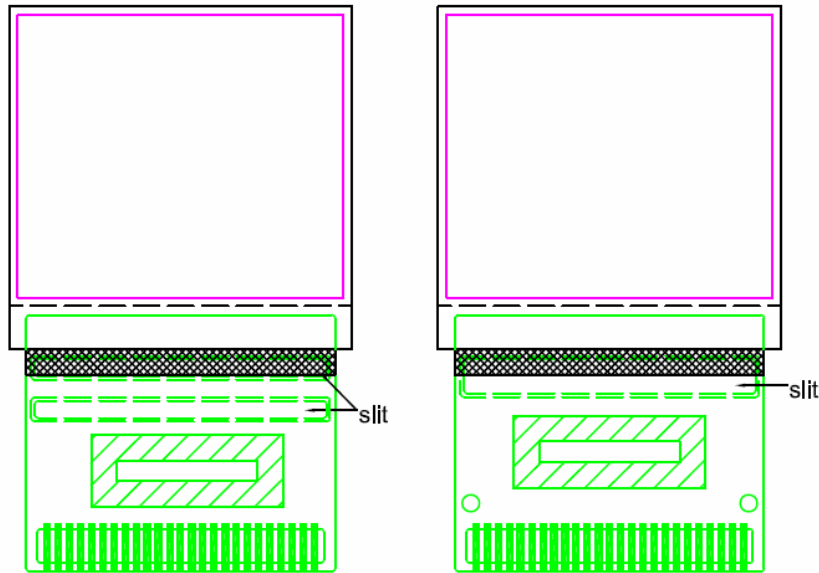
1. When handling the module, wear powder-free antistatic rubber finger cots, and be careful not to bend and twist it.
2. The OLED module is consisted of glass and film, and it should avoid pressure, strong impact, or being dropped from a high position.
3. The OLED module is an electronic component and is subject to damage caused by Electro Static Discharge (ESD). And hence normal ESD precautions must be taken when handling it. Also, appropriate ESD protective environment must be administered and maintained in the production line. When handling and assembling the panel, wear an antistatic wrist strap with the alligator clip attached to the ground to prevent ESD damage on the panel. Antistatic wrist strap should touch human body directly instead of gloves. (See below photos).



4. Take out the panel one by one from the holding trays for assembly, and never put the panel on top of another one to avoid the scratch.
5. Avoid jerk and excessive bend on TAB/FPC/COF, and be careful not to let foreign matter or bezel damage the film.
6. When handling and assembling the module (panel + IC), grab the panel, not the TAB/FPC/COF.
7. Use the tweezers to open the clicks on the connector of PCB before the insertion of FPC/COF, and click them back in. Once the FPC/COF sits properly in the connector, use the tweezers to avoid the damages.

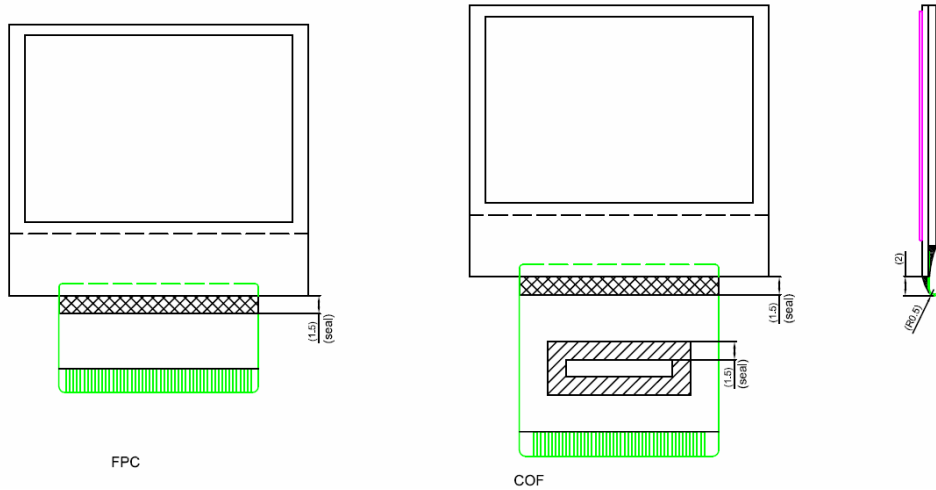


8. Please do not bend the film near the substrate glass. It could cause film peeling and TAB/FPC/COF damage. For TAB, It should bend the slit area as actual OLED it is. For FPC or COF, it is suggested to follow below pictures for instruction (distance between substrate glass and bending area >1.5mm; R>0.5mm).



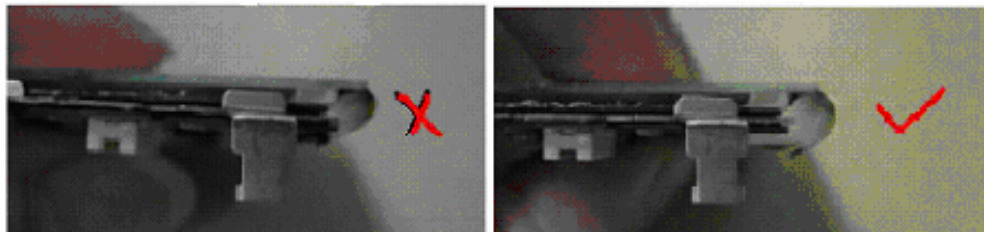
TAB

TAB

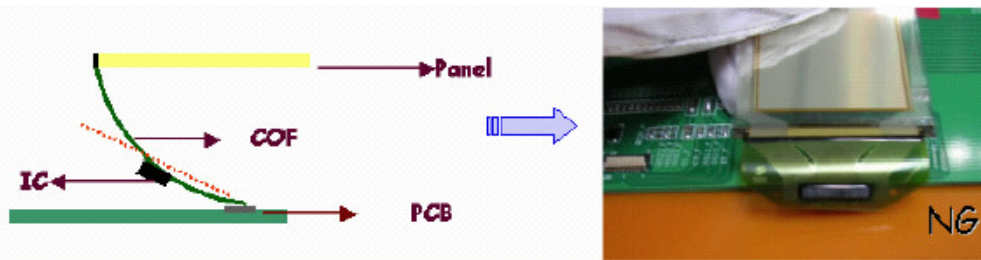
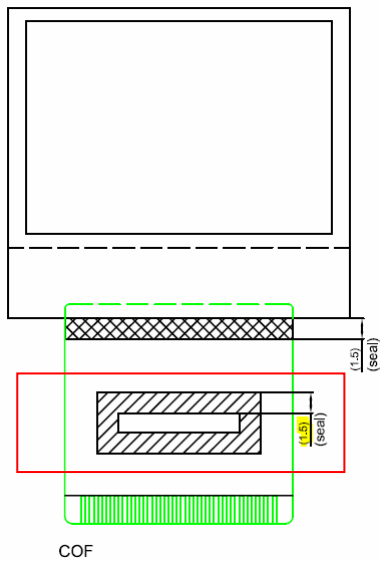


FPC

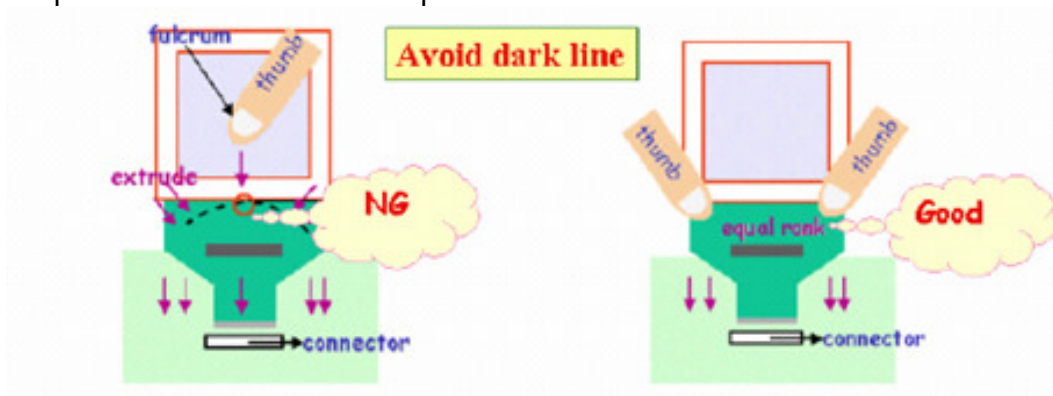
COF



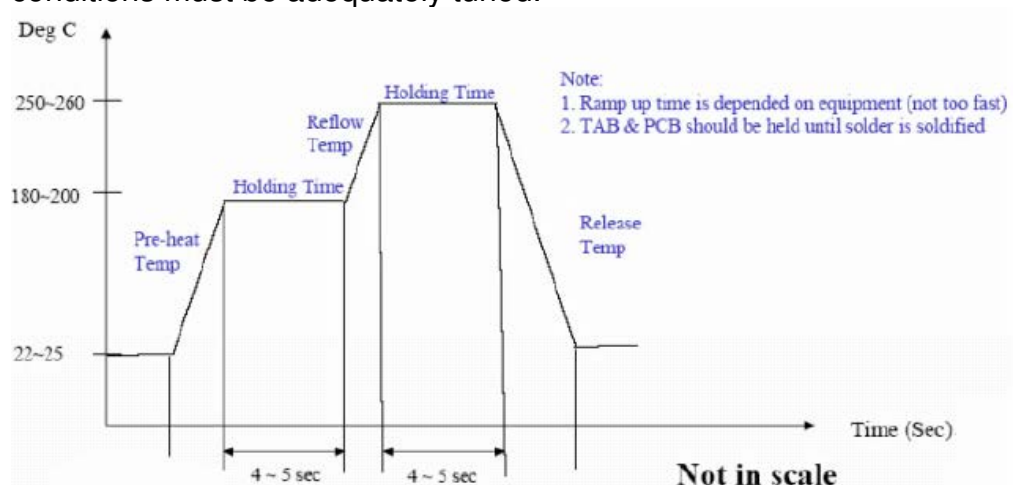
- Avoid bending the film at IC bonding area. It could damage the IC ILB bonding. It should avoid bending the IC seal area. Please keep the bending distance >1.5mm.



- Use both thumbs to insert COF into the connector when assembling the panel. Please refer to the photo.



11. Do not wipe the pin of film and polarizer with the dry or hard materials that will damage the surface. When cleaning the display surface, use the soft cloth with solvent, IPA or alcohol, to clean.
12. Protection film is applied to the surface of OLED panel to avoid the scratch. Please remove the protective film before assembling it. If the OLED panel has been stored for a long time, the residue adhesive material of the protective film may remain on the display surface after remove the protective film. Please use the soft cloth with solvent, IPA or alcohol, to clean.
13. When hand or hot-bar soldering TAB/FPC onto PCB, make sure the temperature and timing profiles to meet the requirements of soldering specification (the specification depends on the application or optimized by customer) to prevent the damage of IC pins by inappropriate soldering.
14. Solder residues arise from soldering process have to be cleaned up thoroughly before the module assembly.
15. Use the voltage and current settings listed in the specification to do the function test after the module assembly.
16. Suggestion for soldering process:
 - i. TAB Lead- free soldering hot bar process
 1. Use pulse heated bonding tool equipment
 2. Material: Sn/Ag/Cu lead-free solder paste with typical 25um thickness on PCB pad. The TAB pin size and shape may be different, please base on the production line to adjust the thickness of PCB pad and temperature.
 3. Bonding Force:--4kg per centimeter square as the starting point.
 4. Suggested bonding tool temperature & time profile is as below for reference. Since there are differences in TAB soldering pins, soldering technicians' skills, mechanism...etc., the soldering conditions must be adequately tuned.



- ii. TAB Lead- free soldering wire process
 - In case of manual soldering (Lead- free solder wire)
 - 1. Solder wire contact iron directly: $280\pm 5^{\circ}\text{C}$ at 3-5secs
 - 2. Solder wire contact TAB lead directly (near iron but not contact): $380\pm 5^{\circ}\text{C}$, 3-5secs
 - 3. Since there are differences in TAB soldering pins, soldering technicians' skills, mechanism...etc., the soldering conditions must be adequately tuned.
- iii. High temperature will result in rapid heat conduction to IC and might cause damage to IC, so please keep the temperature below 380°C . Also, avoid damaging the polyimide and solder resist which might take place at high temperatures. Refold cycles base on the de-soldering status, if the plating of pin was damaged, it can not be used again.

Precautions for Electrical

1. Design using the settings in the specification

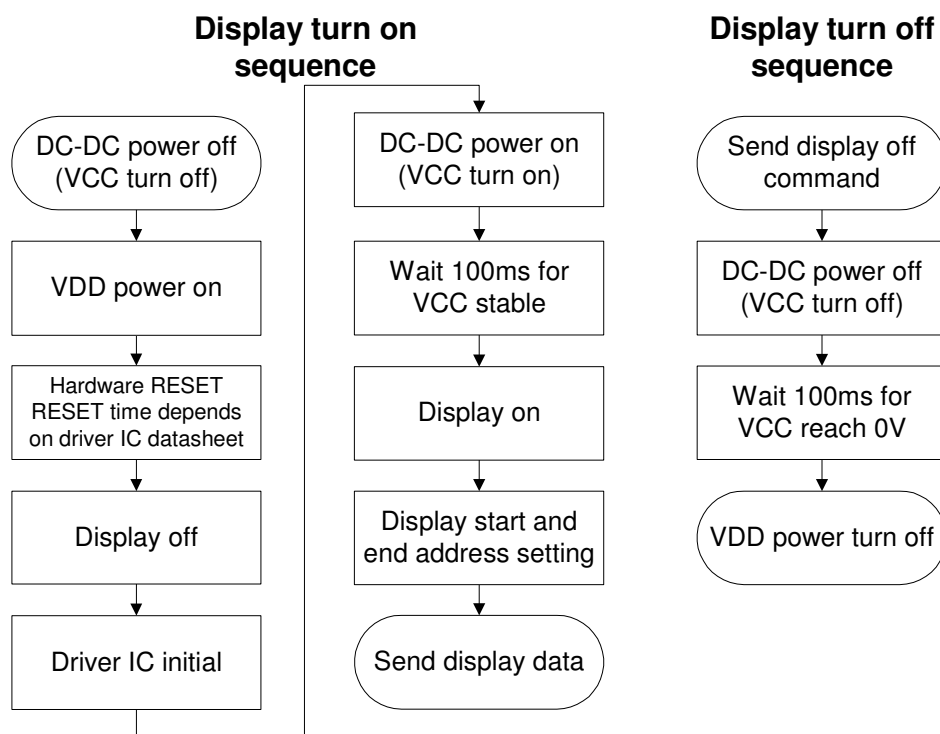
It is very important to design and operate the panel using the settings listed in the specification. It includes voltage, current, frame rate and duty cycle... etc. Operation the OLED outside the range of the specification should be entirely avoided to ensure proper operation of the OLED.

2. Maximum Ratings

To ensure the proper operation of the panel, never design the panel with parameters running over the maximum ratings listed in the specification. Also the logic voltages such as VIL and VIH have to be within the specified range in the specification to prevent any improper operation of the panel.

3. Power on/off procedure

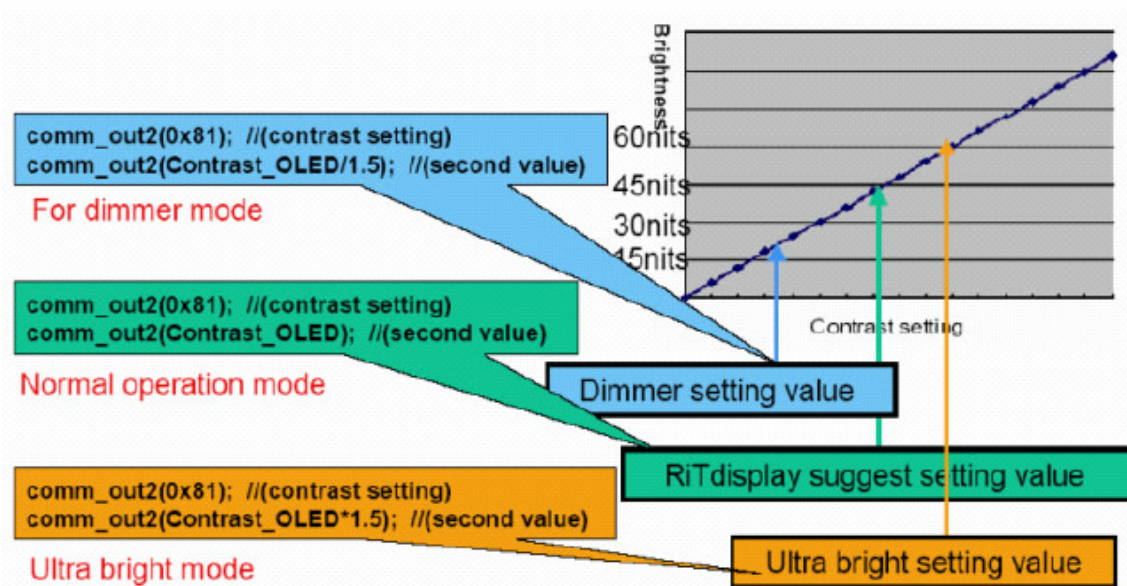
To avoid any inadvertent effects resulting from inappropriate power on/off operations, please follow the directions of power on/off procedure on page 6. Any operation that does not comply with the procedure could cause permanent damage of the IC and should be avoided. When the logic power is not on, do not activate any input signal. Abrupt shutdown of power to the module, while the OLED panel is on, would cause OLED panel malfunction.



4. Power savings

To save power consumption of the OLED, please use partial display or sleep mode when the panel is not fully activated. Also, if possible, make the black background to save power.

The OLED is a self-luminous device and a particular pixel cluster or image can be lit on via software control. So power savings can be achieved by partial display or dimming down the luminance. Depending on the application, the user can choose among Ultra Bright Mode, Normal Operation Mode, and Sleeping Mode. The power consumption is almost in directly proportion to the brightness of the panel, and also in directly proportion to the number of pixels lit on the panel. The customer can save the power by the use of black background and sleeping mode. One benefit from using these design schemes is the extension of the OLED lifetime.



5. Adjusting the luminance of the panel

Although there are a couple of ways to adjust the luminance of the panel, it is strongly recommended that the customer change the contrast setting to adjust the luminance of the panel. Adjusting voltages to achieve desired luminance is not allowed. Be aware that the adjustment of luminance would accompany the change of lifetime of the panel and its power consumption as well.

6. Residual Image (Image Sticking)

The OLED is a self-emissive device. As with other self-emissive device or displays consisting of self-emissive pixels, when a static image frozen for a long period of time is changed to another one with all-pixels-on background, residual image or image sticking is noticed by the human eye. Image sticking is due to the luminance difference or contrast between the pixels that were previously turned on and the pixels that are newly turned on. Image sticking depends on the luminance decay curve of the display. The slower the decay, the less prominent the image sticking is. It is strongly recommended that the user employ the following four strategies to minimize image sticking.

1. Employ image scrolling or animation to even out the lit-on time of each and every pixel on the display, also could use sleeping mode for reduced the residual image and extend the power capacity.
2. Minimize the use of all-pixels-on or full white background in their application because when the panel is turned on full white, the image sticking from previously shown patterns is the most revealing. Black background is the best for power savings, greatest visibility, eye appealing, and dazzling displays.
3. Avoid displaying the characters or menu with high brightness level in a fix position for a long time or repeatedly. If necessary, using the auto fadeout technology.
4. If a static logo is used in the reliability test, change the pattern into its inverse (i.e., turn off the while pixels and turn on the previously unlit pixels) and freeze the inverse pattern as long as the original logo is used, so every pixel on the panel can be lit on for about the same time to minimize image sticking, caused by the differential turn-on time between the original and its reverse patterns.



Scrolling example

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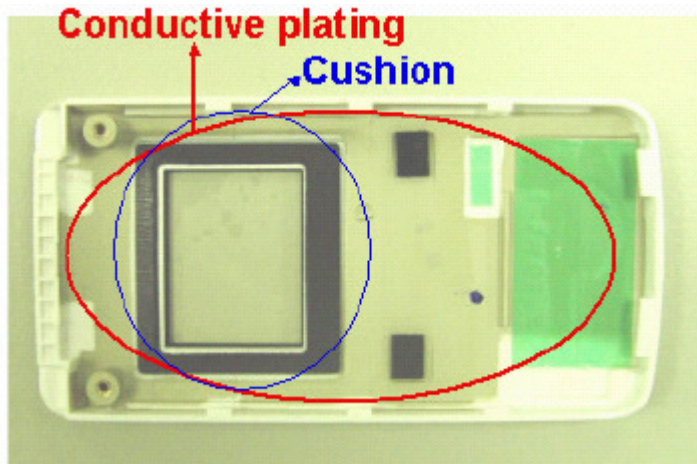
Example: setup and start
comm_out2(0x26); // scrolling setup
comm_out2(0x08); // scrolling numbers/step
comm_out2(0x00); // start page
comm_out2(0x00); // scrolling step/frame
comm_out2(0x08); // end page
comm_out2(0x2F); // start

Example: stop
comm_out2(0x2E); //stop
    
```

Precautions for Mechanical

1. Cushion or Buffer tape on the cover glass

It is strongly recommended to have a cushion or buffer tape to apply on the panel backside and front side when assembling OLED panel into module to protect it from damage due to excessive extraneous forces.



It is recommended that a plating conductive layer be used in the housing for EMI/EMC protection. And, the enough space should be reserved for the IC placement if the IC thickness is thicker than the TAB film when customer design the PCB.

2. Avoid excessive bending of film when handling or designing the panel into the product

The bending of TAB/COF/FPC has to follow the precautions indicated in the specification, extra bending or excessive extraneous forces should be avoided to minimize the chances of film damage. If bending the film is necessary, please bend the designated bending area only. Please refer to items 8 and 9 of Precautions for Handling for more information.

1. Storage

Store the packed cartons or packages at $25^{\circ}\text{C}\pm 5^{\circ}\text{C}$, $55\%\pm 10\%\text{RH}$. Do not store the OLED module under direct sunlight or UV light. For best panel performance, unpack the cartons and start the production of the panels within six months after the reception of them.