128x64
LCD Module Series

GooDisplay®

12864J

Dalian Good Display Co., Ltd.

LCD MODULE SPECIFICATION.

PART NO : YM12864J

FOR MESSRS : _____

CONTENTS

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RECORD OF REVISION

DATE	PAGE	SUMMARY
1998.02.07	ALL	ALL PAGE CHANGED
1998.12.11	5	CHANGE DUTY 1/16 TO DUTY 1/64
2002.08.30	04	4.2 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS SHOCK STORAGE 490.0m/s^2(50G)→ 49.0m/s^2(5G)

3. GENERAL SPECIFICATIONS AND MECHANICAL DATA

3.1 GENERAL SPECIFICATIONS

PLEASE REFER TO :

”CUSTOMER ACCEPTANCE STANDARD SPECIFICATIONS (SP-10-000)”.

3.2 THIS INDIVIDUAL SPECIFICATION IS PRIOR TO GENERAL SPECIFICATIONS.

3.3 MECHANICAL DATA

(1) NUMBER OF DOTS ---------- 128W x 64H DOTS
(2) MODULE SIZE ---------- 93.0W x 70.0H x 14.0T (MAX) mm
(3) VEWING AREA ---------- 70.7W x 38.8H mm
(4) DOT SIZE ---------- 0.48W x 0.48H mm
(5) DOT PITCH ---------- 0.52W x 0.52H mm
(6) VIEWING DIRECTION ---------- 6 O’CLOCK
(7) LED COLOR ---------- YELLOW-GREEN/BLUE-WHITE
(8) LCD COLOR ---------- STN Y-G MODE , TRANSFLECTIVE

4. ABSOLUTE MAXIMUM RATINGS

4.1 ELECTRICAL ABSOLUTE MAXIMUM RATINGS.

ITEM	SYMBOL	MIN.	MAX.	UNIT	COMMENT
POWER SUPPLY FOR LOGIC	VDD-VSS	0	6.0	V	
INPUT VOLTAGE	VI	VSS	VDD	V	
STATIC ELECTRICITY	———	——	100	V	NOTE(1)
POWER SUPPLY FOR LED	VLED-GND	——	6.0	V	

NOTE(1) : TEST METHOD AND CONDITIONS: AFTER CHARGING UP 200PF CAPACITOR BY STATED VOLTAGE , THE CAPACITOR IS CONNECTED WITH INTERFACE PINS OF THE MODULE.

4.2 ENVIRONMENTAL ABSOLUTE MAXIMUM RAINGS.

ITEM	OPERATING		STORAGE		COMMENT
	MIN.	MAX.	MIN.	MAX.	
AMBIENT TEMPERATURE	-20℃	70℃	-30℃	80℃	NOTE(2)
HUMIDITY	NOTE(3)		NOTE(3)		WITHOUT CONDENSATION
VIBRATION	——	4.9 m/s^2 (0.5G)	——	19.6 m/s^2 (2G)	10~300Hz XYZ DIRECTIONS 1Hr EACH
SHOCK	——	29.4 m/s^2 (3G)	——	49.0 m/s^2 (5G)	10mS XYZ DIRECTIONS 1 TIME EACH
CORROSIVE GAS	NOT ACCEPTABLE		NOT ACCEPTABLE		

NOTE(2) : Ta AT -20℃ : 48HR MAX.
Ta AT 60℃ : 168HR MAX.

NOTE(3) : Ta ≦ 40℃ : 90% RH MAX.
Ta ＞ 40℃ : ABSOLUTE HUMIDITY MUST BE LOWER THAN THE HUMIDITY OF 90%RH AT 40℃. (50% RH AT 50℃)

5. ELECTRICAL CHARACTERISTICS

Ta = 25℃ VDD = 5.0±0.25V

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
LOGIC CIRCUIT POWER SUPPLY VOLTAGE	VDD-VSS	———	4.75	5.0	5.25	V
INPUT VOLTAGE	VOH	NOTE (1)	0.7*VDD	——	VDD	V
INPUT VOLTAGE	VOL	NOTE (1)	GND	——	0.3*VDD	V
LOGIC CIRCUIT POWER SUPPLY CURRENT	IDD	VDD-VSS=5.0V	——	——	6.0	mA
RECOMMENDED LCD DRIVING VOLTAGE (NOTE 2)	VDD - VO DUTY = 1/64 φ = 10°	Ta = 0℃	——	9.4	——	V
		Ta = 25℃	——	9.0	——	V
		Ta = 50℃	——	8.7	——	V
THE POWER SUPPLY FOR LED	ILED	VLED=5.0V	——	360	——	mA

NOTE(1) : CS1 , CS2 , R/W , D/I , DB0~DB7 , E , RST

NOTE(2) : RECOMMENDED LCD DRIVING VOLTAGE MAY FLUCTUATE ABOUT ± 0.5V BY EACH MODULE.

6. OPTICAL CHARACTERISTICS.

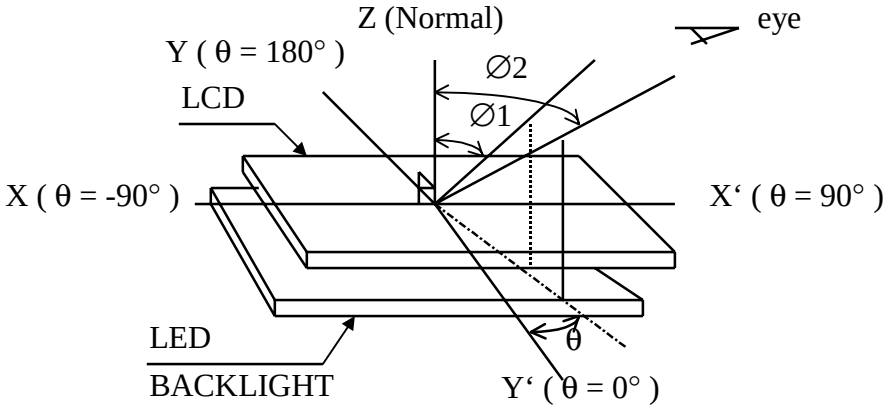
Ta = 25°C VDD = 5.0V ± 0.25V

I T E M	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	NOTE
VIEWING AREA	Φ2-Φ1	K≧ 1.4	20	——	——	deg.	1
CONTRAST RATIO	K	Φ = 10° θ = 0°	2	——	——	——	2,3
RESPONSE TIME	tr(rise)	Φ = 10° θ = 0°	——	250	400	ms	4
	tf(fall)	Φ = 10° θ = 0°	——	250	400	ms	4
THE BRIGHTNESS OF BACKLIGHTING SOURCE	——	(*) φ = 0° θ = 0°	4.0	——	——	cd/m^2	5,6

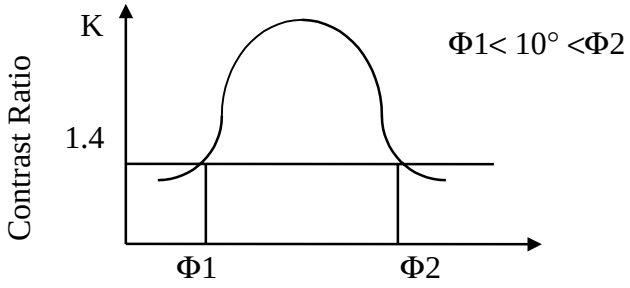
(* UNDER NORMAL TEMPERATURE AND HUMIDITY IN A DARK ROOM)

NOTE (6) : DOT-MATRIX TYPE LED BACKLIGHT.
NOTE (7) : SIDE LED BACKLIGHT.

NOTE (1) : DEFINITION OF θ AND Φ



NOTE (2) : DEFINITION OF VIEWING ANGLE Φ1 AND Φ2

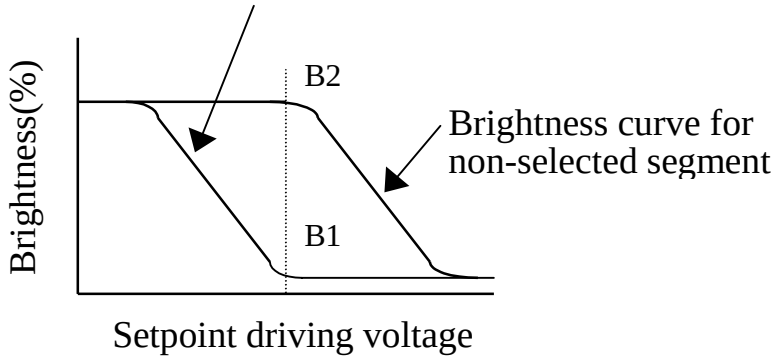


Viewing Angle

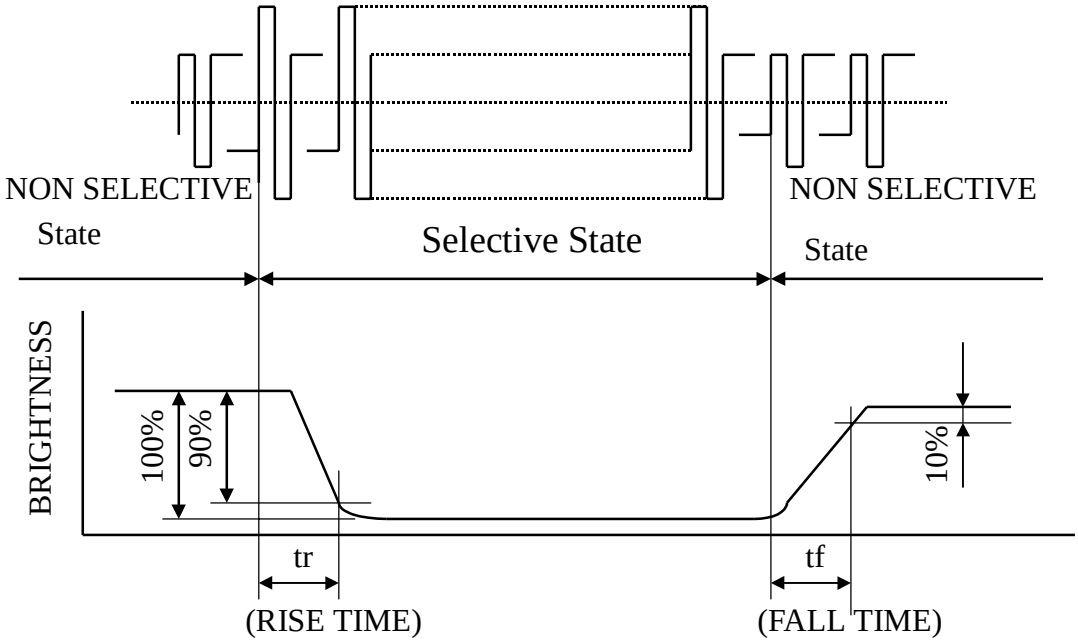
NOTE (3) : DEFINITION OF CONTRAST“K”

$$K = \frac{\text{Brightness of non-selected segment (B2)}}{\text{Brightness of selected segment (B1)}}$$

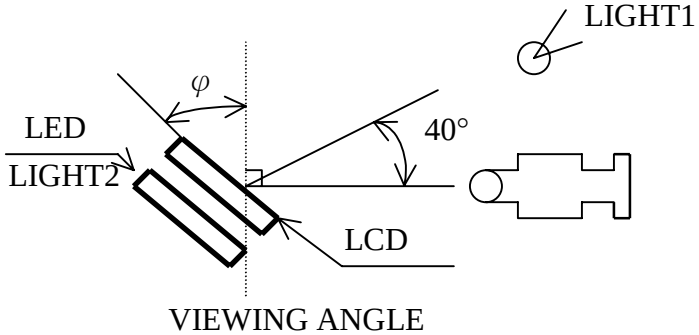
Brightness curve for selected segment



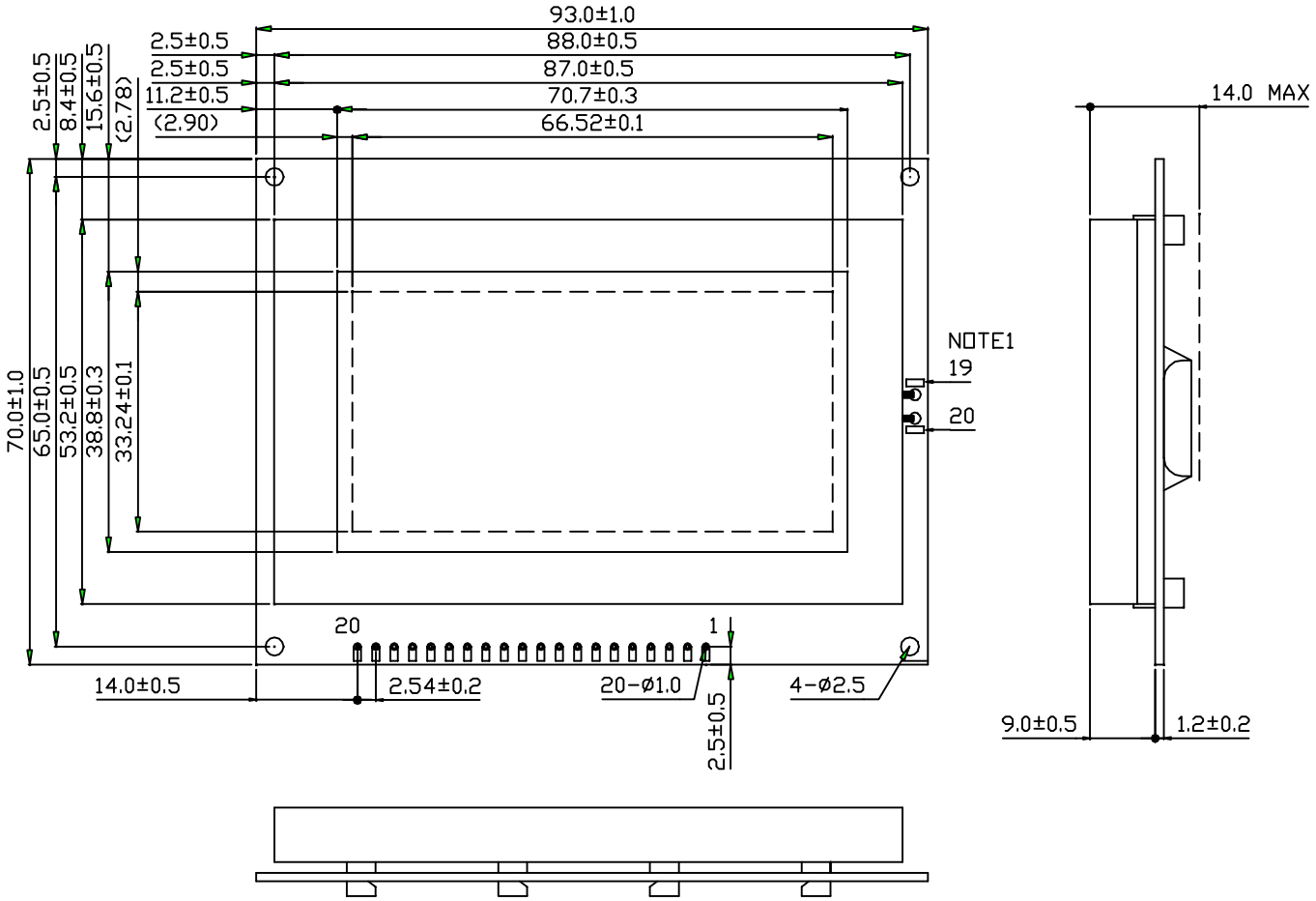
NOTE(4) : DEFINITION OF OPTICAL RESPONSE



NOTE (5) : POSITION OF LIGHT



7. OUTLINE DIMENSION.

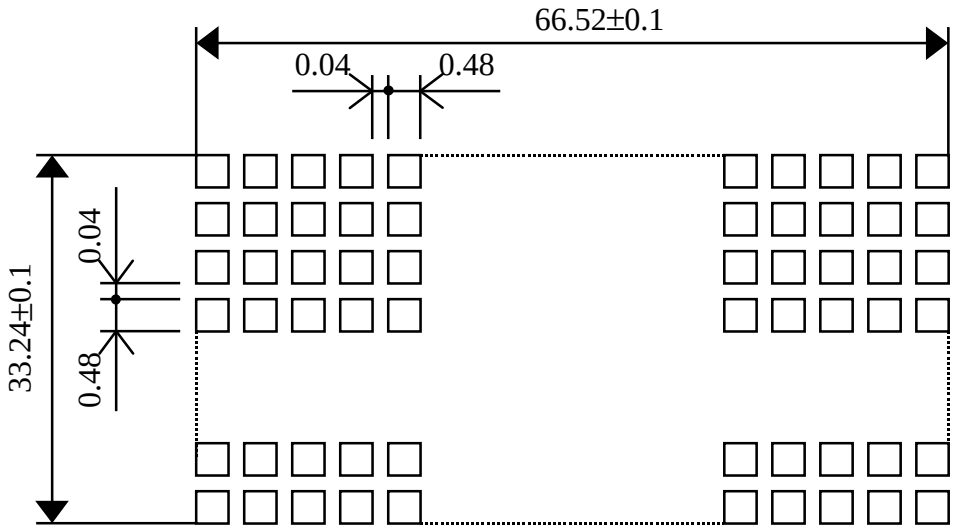


6 O'CLOCK

NUIT : mm
SCALE : NTS

NOTE1 : POWER SUPPLY FOR LED B.L

NOTE 1. DETAIL DRAWING OF MATRIX PATTERN



NOT SPECIFIED TOLERANCE: ±0.01mm

NOTE 2 . INTERNAL PIN CONNECTION

PIN NO	SYMBOL	LEVEL	FUNCTION
1	VSS	——	GROUND
2	VDD	——	POWER SUPPLY FOR LOGIC CIRCUIT(+5V)
3	VO	——	OPERATING VOLTAGE FOR LCD DRIVING(13V)
4	D/I	H/L	H : DATA INPUT L : INSTRUCTION CODE INPUT
5	R/W	H/L	H : DATA READ (LCD MODULE → MPU) L : DATA WRITE (LCD MODULE ← MPU)
6	E	H,H→L	ENABLE SINGNAL
7 | 14	DB0 | DB7	H/L	DATA BUS LINE
15	CS1	H	CHIP SELECTION FOR IC1
16	CS2	H	CHIP SELECTION FOR IC2
17	$\overline{RST}$	L	RESET
18	VOUT	——	POWER SUPPLY FOR LCD DRIVING (-10V)
19	VLED+	——	POWER SUPPLY FOR LED BACKLIGHT(+5V)
20	VLED-	——	POWER SUPPLY FOR LED BACKLIGHT

NOTE 3 : TIMING CHARACTERISTICS

Item	Symbol	Min..	Typ.	Max.	Unit	Fig.
E cycle time	t_{CYC}	1000	--------	--------	ns	1 , 2
E high level width	P_{WEH}	450	--------	--------	ns	1 ,2
E low level width	P_{WEL}	450	--------	--------	ns	1 , 2
E rise time	t_r	--------	--------	25	ns	1 ,2
E fall time	t_f	--------	--------	25	ns	1 , 2
Address setup time	t_{AS}	140	--------	--------	ns	1 ,2
Address hold time	t_{AH}	10	--------	--------	ns	1 ,2
Data setup time	t_{DSW}	200	--------	--------	ns	1
Data delay time	t_{DDR}	--------	--------	320	ns	2
Data hold time (Write)	t_{DHW}	10	--------	--------	ns	1
Data hold time (Read)	t_{DHR}	20	--------	--------	ns	2

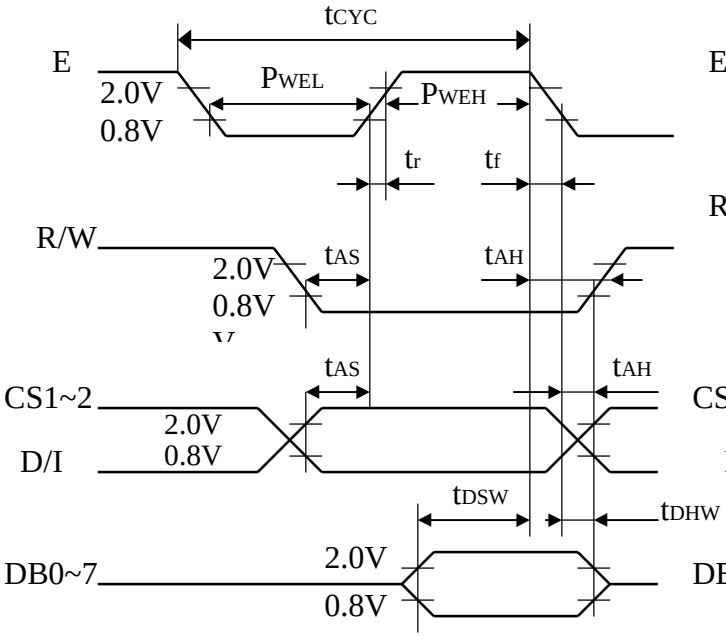


Fig . 1 CPU Write Timing

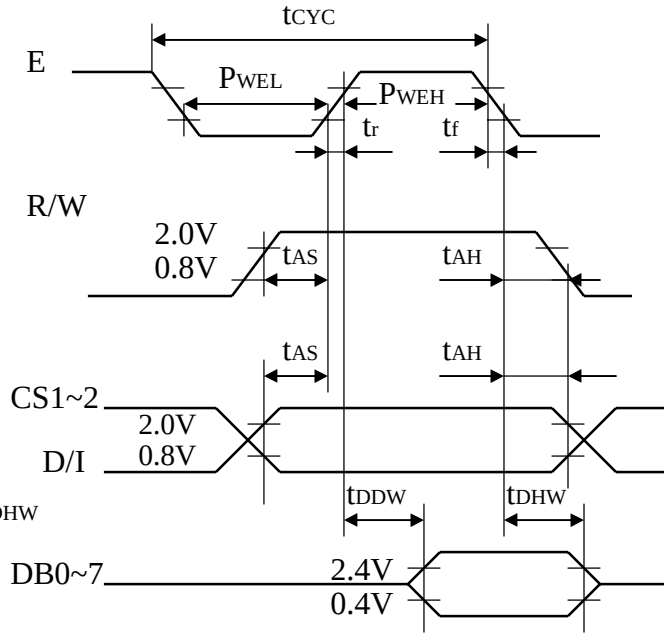
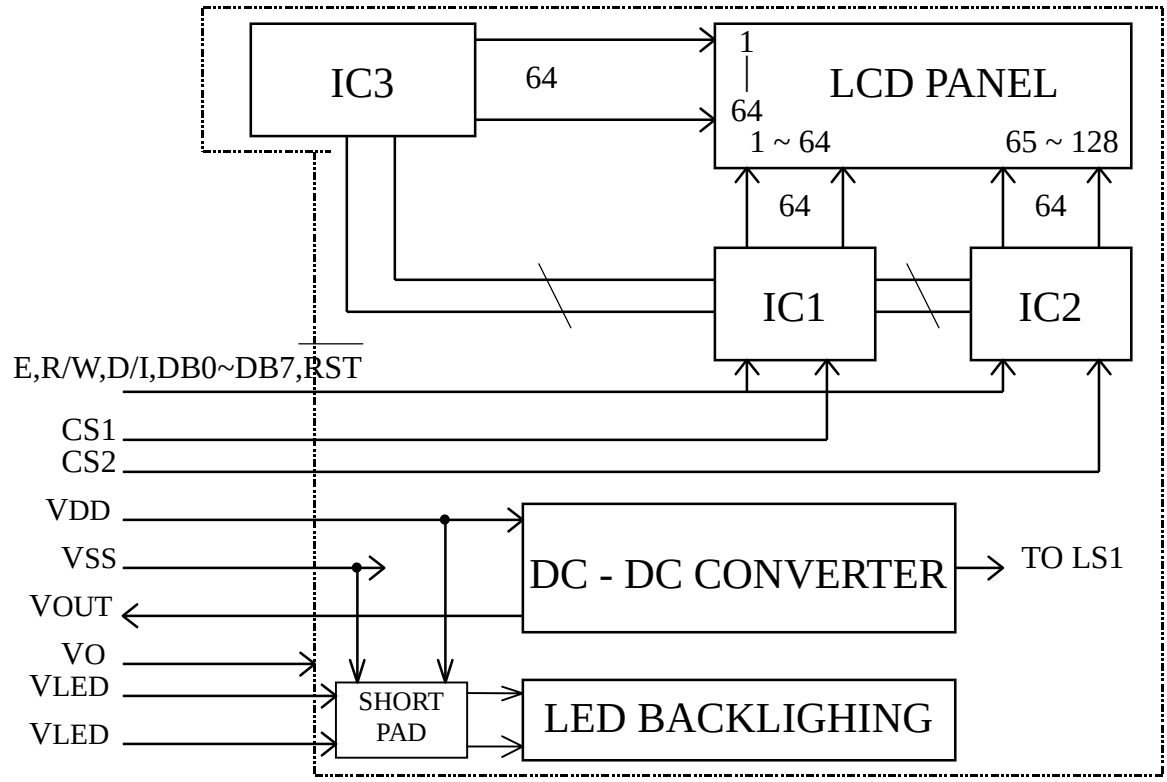


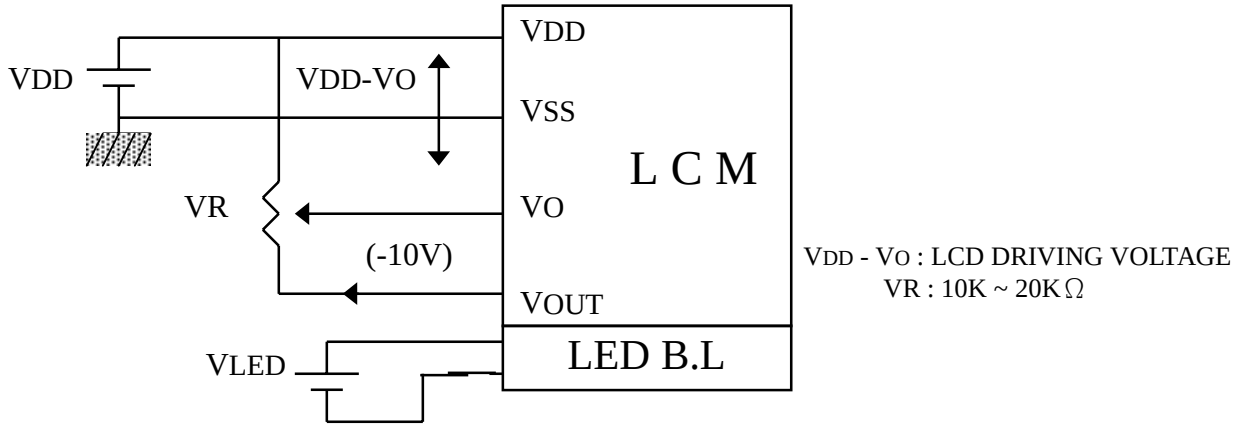
Fig . 2 CPU Read Timing

8. BLOCK DIAGRAM AND POWER SUPPLY

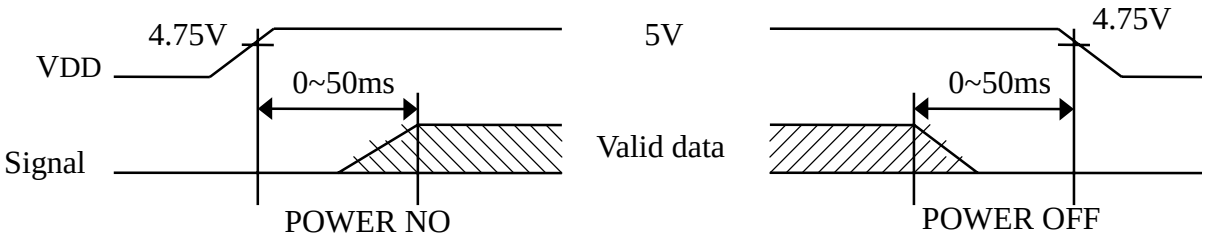
8.1 BLOCK DIAGRAM



8.2 POWER SUPPLY FOR LCM



8.3 POWER AND INTERFACE TIMING SEQUEN



♡ FUNCTION OF EACH BLOCK

●Interface Control

(1) I/O buffer

Data is transferred through 8 data buses (DB0~DB7).

DB7 . . . MSB (Most significant Bit)

DB0 . . . LSB (Least significant Bit)

Data can neither be input nor output unless CS1 to CS2 are in the active mode. Therefore , when CS1 to CS2 are not in active mode it is useless to switch the signals of input terminals except RST and ADC, namely, the internal state is maintained and no instruction excute. Besides, pay attention to RST and ADC which operate irrespectively by CS1 to CS2 .

(2) Register

Both input register and output register are provided to interface to MPU of which the speed is different from that fo internal operation. The selection of these registers depend on the combination of R/W and D/I signals.

D/I	R/W	Operation
1	1	Reads data out of output register as internal operation (display data RAM → output register)
1	0	Writes data into input register as internal operation (input register → display data RAM)
0	1	Busy check. Read of status data.
0	0	Instruction

(1) Input register

Input register is used to store data temporarily before writing it into display data RAM.

The data from MPU is written into input register, then into display data RAM automatically by internal operation.

When CS1 to CS2 are in the active mode and D/I and R/W select the input register as shown in Table 1, data is latched at the fall of E signal.

(2) Output register

Output register in used to store data temporarily which is read from display data RAM. To read out the data from output register, CS1 to CS2 should be in the active mode and both D/I and R/W should be 1. With READ instruction, data stored in the output register is output while E is . “H” level. Then , at the fall of E, the display data at the indicated address is latched into the output register and the address in increased by 1.
The contents in the output register is rewritten with READ instruction, while is held with address set instruction, etc.

Therefore, the data of the specified address can not be output with READ instruction soon after the address is set, but can be output at the second read of data. That is to say, one dummy read is necessary. Fig.5 shows the CPU read timing.

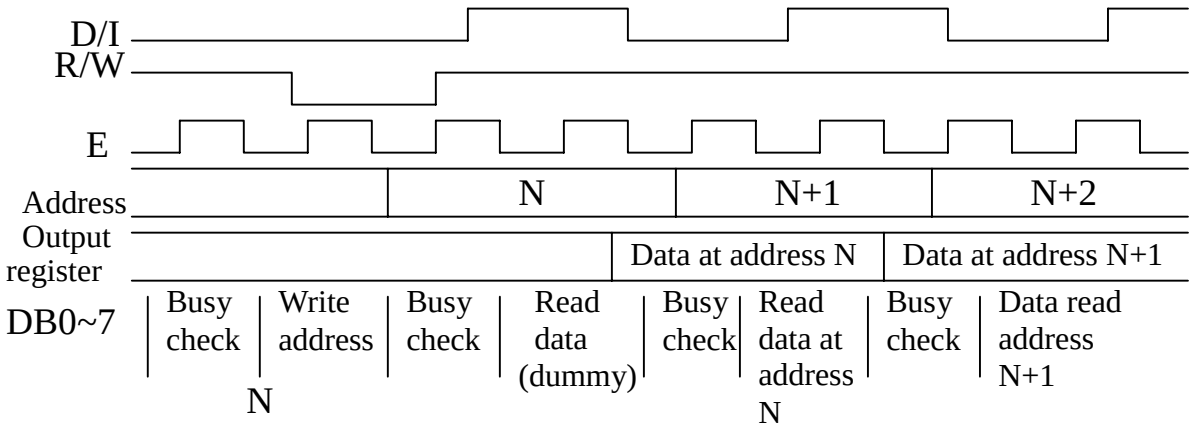
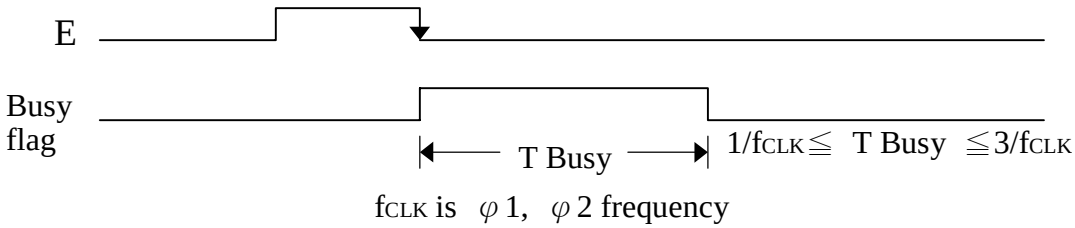


Fig.5 CPU Read Timing

● Busy Flag

“1” of busy flag indicates that HD61202 is on the move and any instructions except Status Read instruction can not be accepted. The value of the busy flag is read out on DB7 by the Status Read instruction . Make sure that the busy flag is reset (“0”) before the issue of instruction.



- Display ON/OFF Flip Flop

  Display ON/OFF flip flop selects one of two states, ON state and OFF state of segments Y1 to Y64 . In ON state, the display data corresponding to that in RAM is output to the segments. On the other hand, the display data at all segments disappear in OFF state independent of the data in RAM. It is controlled by display ON/OFF Instruction '0' of RST signal sets the segments in OFF state. The status of the flip flop is output to DB5 by Status Read instruction . Display ON/OFF instruction does not influence data in RAM. To control display data latch by this flip flop, CL signal (display synchronous signal) should be input correctly.

- Display Start Line Register

  The register specifies a line in RAM which corresponds to the top line of LCD panel , when displaying contents in display data RAM on the LCD panel . It is used for scrolling of the screen .
  6-bit display start line information is written into this register by display start line set instruction, with 'H' level of FRM signal instructing to start the display , the information in this register is transferred to z address counter which controls the display address , and the z address counter is preset.

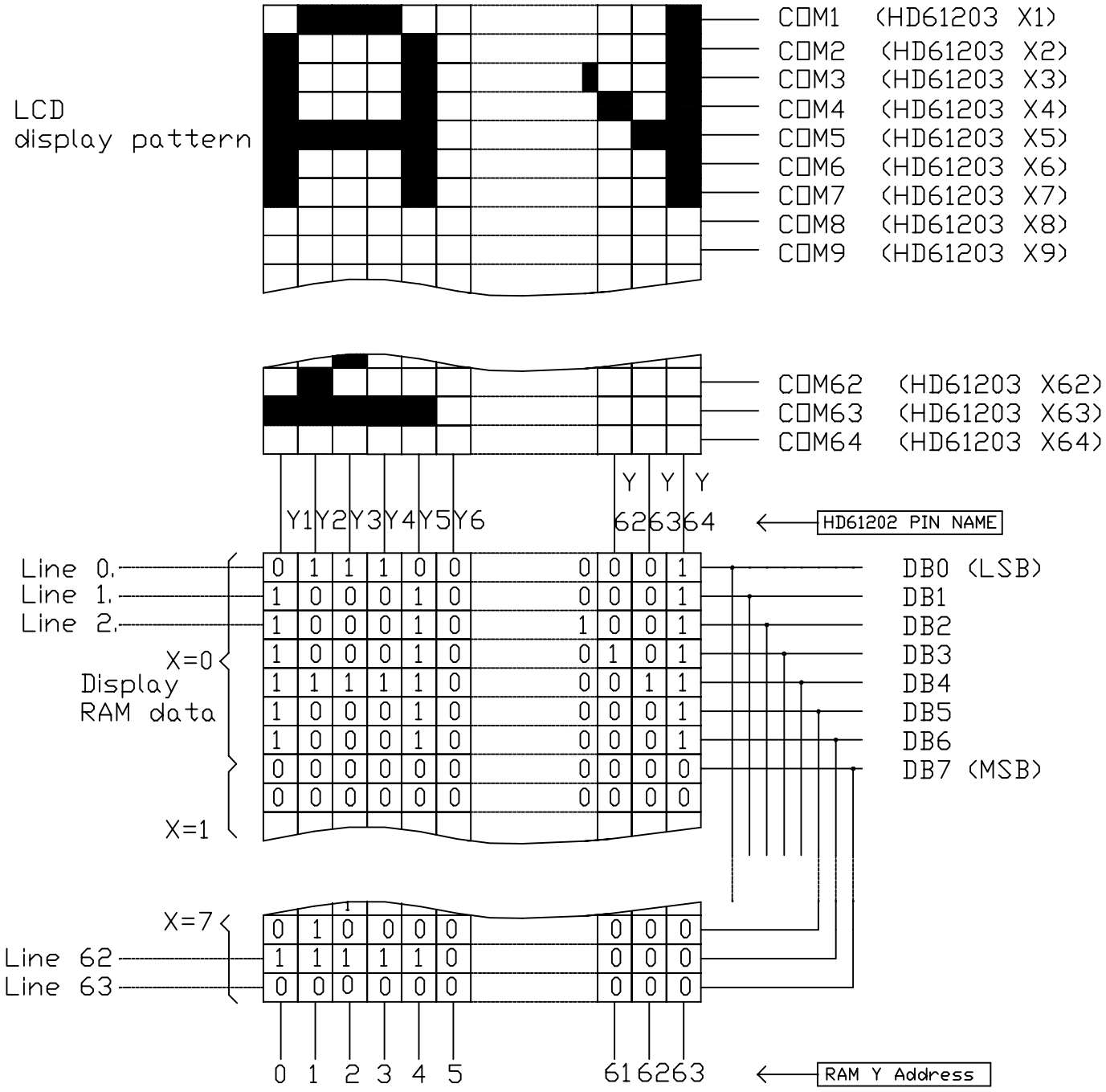
- X,Y Address counter

  This is a 9-bit counter which designates addresses of internal display data RAM. X address counter of upper 3 bits and Y address counter of lower 6 bits should be set each address by respective instruction.

  (1) X address counter
  Ordinary register with no count functions. An address is set in by instructions .
  (2) Y address counter
  An address is set in by instruction and it is increased by 1 automatically by R/W operations of display data. The Y address counter loops the values of 0 to 63 to count.

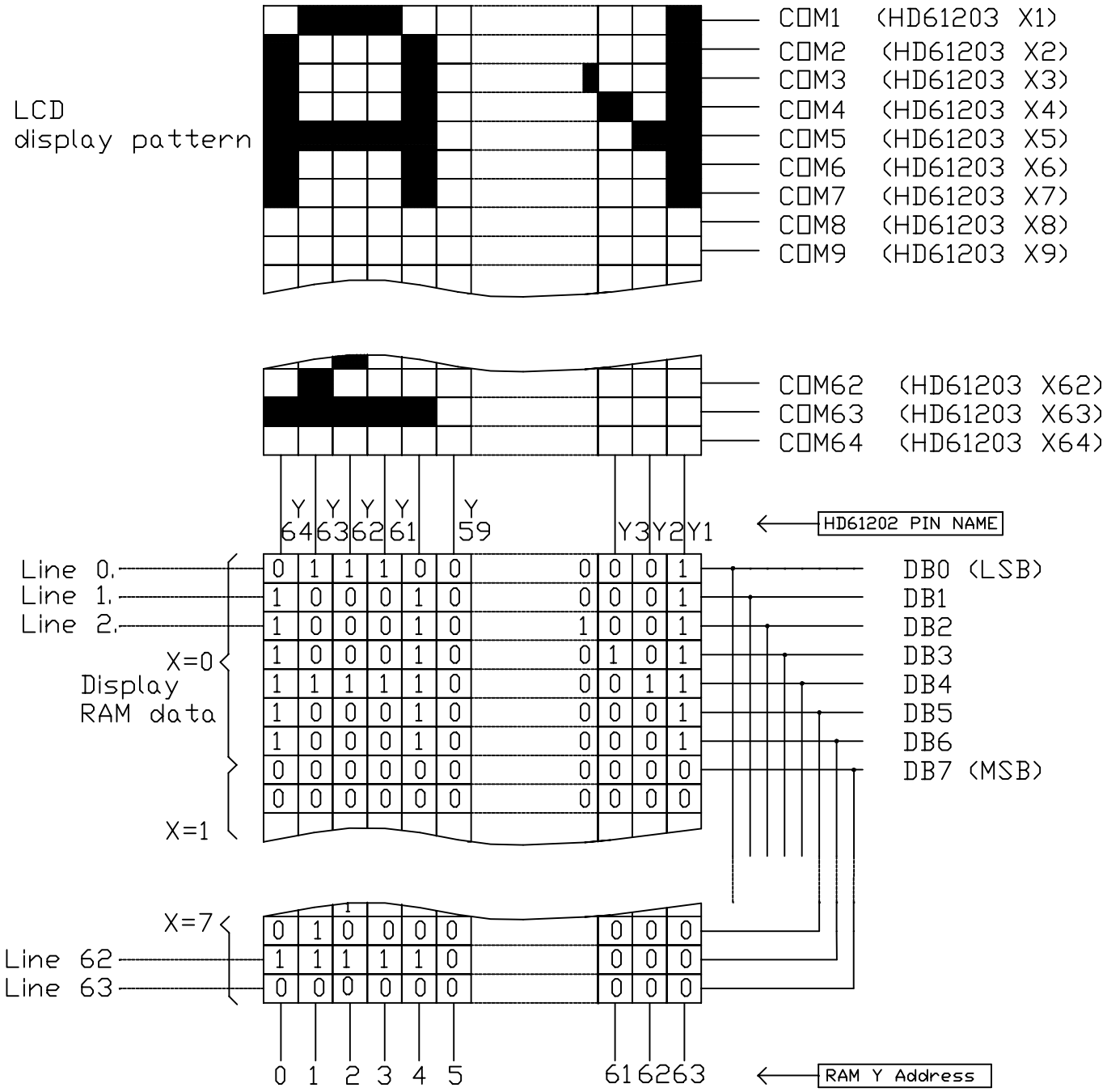
- Display Data RAM

Dot data for display is stored in this RAM. 1-bit data of this RAM corresponds to light ON (data=1) and light OFF (data=0) of 1 dot in the display panel . The correspondence between Y address of RAM and segment PINs can be reversed by ADC signal (ADC is terminal NO.1)
As ADC signal controls Y address counter , a reverse of the signal during the operation causes malfunction and destruction of the contents of register and data of RAM. Therefore never fail to connect ADC pin to VCC or GND when using.
Fig.6 shows the relations between Y address of RAM and segment pins in the cases of ADC= 1 and ADC=0. (display start line = 0, 1-64 duty.)



(a) ADC="1" (Connected to Vcc)

Fig. 6 Relation between RAM Data and Display



(a) ADC="0" (Connected to GND)

Fig. 6 Relation Between RAM Data and Display

● Z Address Counter

The Z address counter generates address for outputting the display data synchronized with the common signal . This counter consists of 6 bit and counts up at the fall of CL signal . With “H” level of RAM, the contents of the display start line register is preset at the Z counter.

● Display data Latch

The display data latch stores the display data temporarily which is output from display data RAM to liquid crystal driving circuit.
Data is latched at the rise of CL signal. Display ON/OFF instruction controls the data in this latch and does not influence data in display data RAM.

● Liquid Crystal Display Circuit

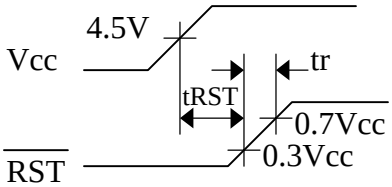
The combination of latched display data and M signal causes one of the 4 liquid crystal driver lives, V1,V2,V3 and V4 to be output.

● Reset

The system can be initialized by setting RST termianl at “LOW” level when turning power ON.
(1) Display-OFF
(2) Set display start line register 0 line.
While RST is in Low level , any instruction except Status Read cannot be accepted. Therefore, Carry out other instructions after making sure that DB4=0 (clear RESET) and DB7=0 (Ready) by Status Read instruction.
The conditions of Power Supply at initial power up are as follows.

Item	Symbol	Min.	Typ.	Max.	Unit
Reset time	tRST	1.0	-------	-------	us
Rise time	tr	-------	-------	200	ns

Do not fail to set the system again because RESET during operation may destroy the data in all the register except ON/OFF register and in RAM.



■ Display Control Instructions

● Outline

Table 2 shows the instructions. Read/Write (R/W) signal, Data/Instruction (D/I) signal and Data bus signal (DB0 to DB7) are also called instructions because the internal operation depends on the signals from MPU. These explanations are detailed from the following page. Generally, there are following three Kinds of instructions.

(1) Instruction to give address in the internal RAM
(2) Instruction to transfer data from/to the internal RAM
(3) Other instructions

In general use, the instruction (2) are used most frequently. But, since Y address of the internal RAM is increased by 1 automatically after writing (reading) data, the program can be lessened. During the execution of an instruction, the system cannot accept other instructions than Status Read instruction. Send instructions from MPU after making sure if the busy flag is “0” , which is the proof an instruction is not being excuted.

Table 2. Instructions

Instructions	Code										Functions	
	R/W	D/I	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
1. Display ON/OFF	0	0	0	0	1	1	1	1	1	1/0	Controls the ON/OFF of display. RAM data and Internal status are not affected. 1: NO, 0:OFF.	
2. Display start line	0	0	1	1	Display start line (0 ~ 63)						Specifies a RAM line display at the top of the screen.	
3. Set page (X address)	0	0	1	0	1	1	1	Page (0 ~ 7)			Sets the page (X address) of RAM at the page (X address) register.	
4. Set Address	0	0	0	1	Y address (0 ~ 63)						sets the Y address at the Y address counter	
5. Status Read	1	0	Busy	0	ON / OFF	RESET	0	0	0	0	Reads the status. RESET 1:reset 0:nornal NO/OFF 1:display OFF 0:display ON Busy 1:on the internal operation 0:Ready	
6. Write display data	0	1	Write Data								Writes data DB0 (LSB) to (DB7) (MSB) on the data bus into display RAM.	Has access to The address of The display RAM specified In advance. After the access, Y address is Increased by 1.
7. Read display data	1	1	Read Data								Reads data DB0 (LSB) to DB7 (MSB) from the display RAM to the data bus.	

(Note 1) Busy time varies with the frequency (fCLK) of ϕ1,and ϕ2.
(1/fCLK≦TBUSY≦3/fCLK)

■ Detailed Explanation

(1) Display ON/OFF

	R/W	D/I	DB7							DB0
Code	0	0	0	0	1	1	1	1	1	D

←high—order—bit low—order—bit→

The display data appears when D is 1 and disppears when D is 0. Though the data is not on the screen width D=0 , it remains in the display data RAM. Therefore, you can make it appear by changing D=0 into D=1.

(2) Display start line

	R/W	D/I	DB7							DB0
Code	0	0	1	1	A	A	A	A	A	A

←high—order—bit low—order—bit→

Z address AAAAA (binary) of the display data RAM is set at the display start line register and displayed at the top of the screen. Fig. 7 are the examples of display (1/64 duty) when the start line=0~3. When the display duty is 1/64 or more (ex. 1/32, 1/24 etc.) the data of total line number of LCD screen, from the line specified by display start line instruction, is displayed.

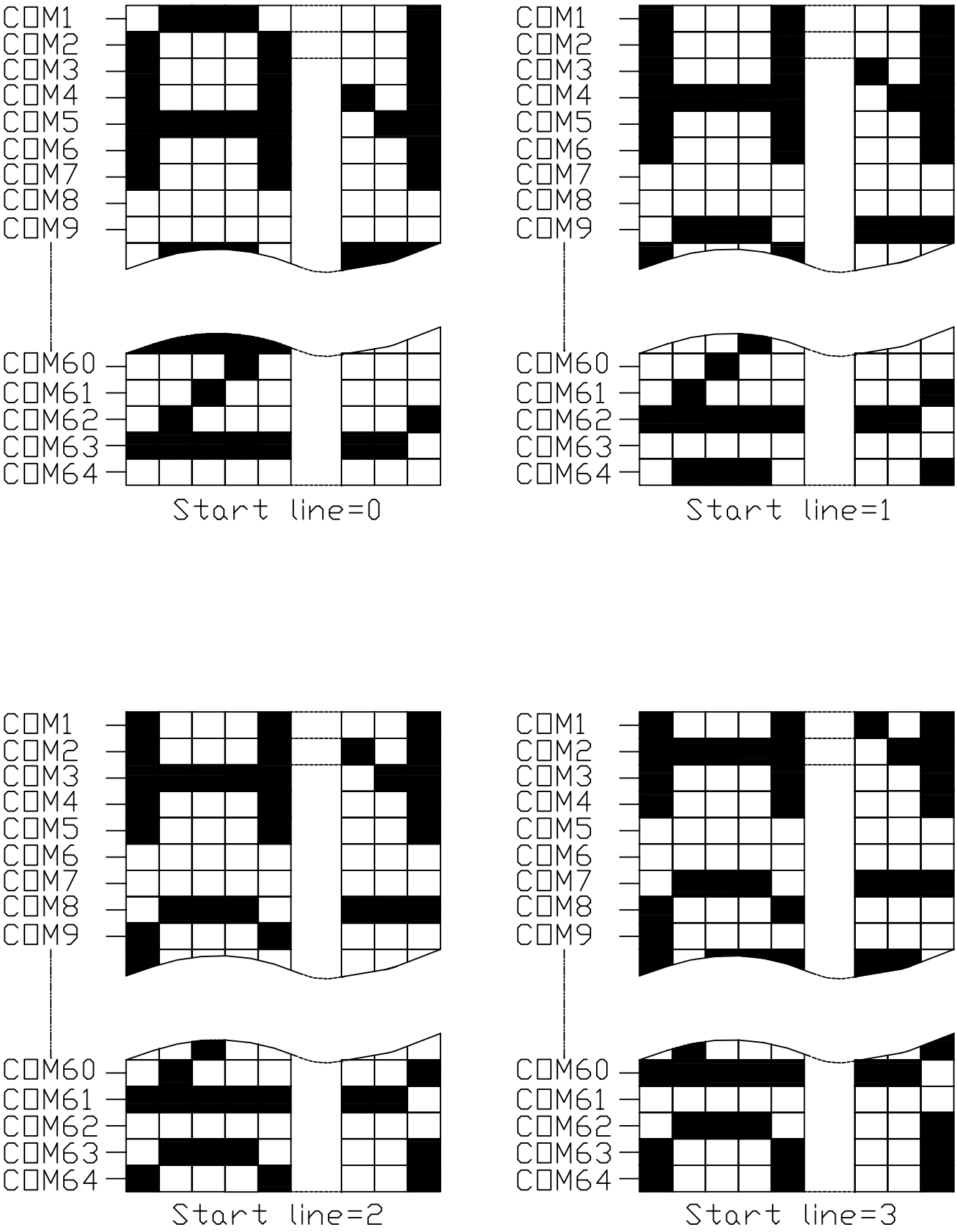


Fig.7 Relation Between Start Line and Display

(3) Set page (X address)

	R/W	D/I	DB7							DB0
Code	0	0	1	0	1	1	1	A	A	A

←high—order—bit low—order—bit→

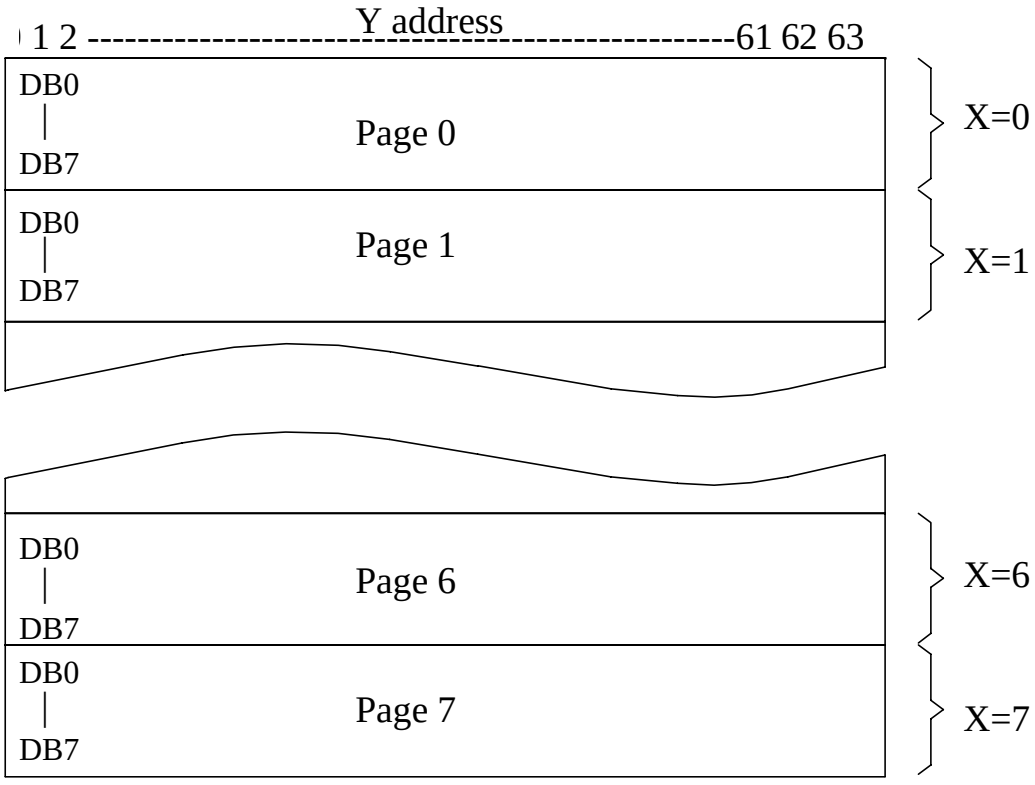
X address AAA (binary) of the display data RAM is set at the X address register. After that, writing or reading to or from MPU is executed in this specified page until the next page is set.

(4) Set Y address

	R/W	D/I	DB7							DB0
Code	0	0	0	1	A	A	A	A	A	A

←high—order—bit low—order—bit→

Y address AAAAAA (binary) of the display data RAM is set at the Y address counter. After that, Y address counter is increased by 1 every time the data is written of read to or from MPU.



Fig, 8 Address Configuration of Display Data RAM

(5) Status Read

	R/W	D/I	DB7							DB0
Code	1	0	BUSY	0	ON/OFF	RESET	0	0	0	0

←high—order—bit low—order—bit→

BUSY : When BUSY is 1, the LSI is in internal operation. NO instructions are accepted while BUSY is 1, so you should make sure that BUSY is 0 before writing the next instruction

ON/OFF : This bit shows the liquid crystal display conditions - NO condition or OFF condition.
When ON/OFF is 1, the display is in OFF condition.
When ON/OFF is 0, the display is in ON condition.

RESET : RESET=1 shows that the system is being initialized. In this condition, any instructions except Status Read instruction cannot be accepted.
RESET=0 shows that initializing has finished and the system is in the usual operation.

(6) Write Display Data

	R/W	D/I	DB7							DB0
Code	0	1	D	D	D	D	D	D	D	D

←high—order—bit low—order—bit→

Writes 8-bit data DDDDDDDD (binary) into the display data RAM.
The Y address is increased by 1 automatically.

(7) Read Diaplay Data

	R/W	D/I	DB7							DB0
Code	1	1	D	D	D	D	D	D	D	D

←high—order—bit low—order—bit→

Read out 8-bit data DDDDDDDD (binary) from the display data RAM. Then Y address is increased by 1 automatically.
One dummy read is necessary soon after the address setting. For details, refer to the explanation of output register in “FUNCTION OF EACH BLOCK”.